Transactions on Machine Intelligence 6(1) (2023) 41-52

ISSN Online: 2821-1693

Transactions on Machine Intelligence

Journal Homepage: https://tmachineintelligence.ir/index.php/TMI

# High efficiency nonvolatile D Flip-Flop

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**ARTICLE INFO**

Article History:
Received 8 December 2022
Received in revised form 14 February 2023
Accepted 28 March 2023
Available online 28 March 2023

Keywords:
MTJ Device, Flip-Flops, Power Gating, Non-Volatile Memory Systems

**ABSTRACT**

As semiconductor technologies continue to advance, the persistent trend of transistor miniaturization introduces significant design challenges, particularly regarding power dissipation. Among the most impacted components are flip-flops essential building blocks in digital circuits whose energy efficiency becomes increasingly critical in ultra-scaled technologies. To address this, engineers have explored power-saving techniques such as selective circuit deactivation during idle periods. While effective in reducing power consumption, such methods often come at the cost of data volatility and potential information loss. To mitigate these drawbacks, recent research has focused on the integration of non-volatile elements into conventional flip-flop designs. A promising solution lies in the use of Magnetoresistive Tunnel Junctions (MTJs), which offer non-volatility along with high switching speeds and reduced power requirements. MTJ-based designs enable circuits to retain data even when powered down, thereby eliminating the need for constant power supply while ensuring data integrity. This study proposes a non-volatile flip-flop architecture leveraging MTJ technology, demonstrating marked improvements over conventional volatile counterparts. Through extensive simulations and comparative analyses, the proposed design achieves substantial gains in key performance metrics: a reduction of up to 54% in write energy, a 5% improvement in clk-to-q delay, and a 17% enhancement in the power-delay product (PDP). These advancements underscore the viability of MTJ-based flip-flops as a robust, energy-efficient alternative for next-generation low-power, high-performance integrated circuits.

## 1. INTRODUCTION

The field of nonvolatile flip-flops (NVFFs) has seen significant advancements in recent years, with a focus on improving efficiency and reliability. Morsali (2021) introduced a high-speed and low-power spintronic-based NVFF, which uses the spin Hall effect-assisted spin-transfer torque magnetic tunnel junction (SHE-assisted STT-MTJ) to provide nonvolatile data storage [1]. This design is particularly notable for its ability to facilitate power gating and dual-supply techniques, making it suitable for ultra-energy-efficient integrated circuits. Natsui (2021) further enhanced the reliability of NVFFs by proposing a design that can detect arbitrary errors during data storage, addressing a key challenge in nonvolatile power gating [2]. Kim (2021) focused on improving the area,

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http://dx.doi.org/10.47176/TMI.2023.41

power, and speed of NVFFs by introducing two novel FeFET-based designs. These designs offer better performance than previous FeFET-based NVFFs, making them promising candidates for energy-efficient applications [3].

Lastly, Alghareb (2019) presented an energy-efficient magnetic NVFF, which achieved significant reductions in power consumption, backup energy, and restore energy compared to other NVFFs [4].

These studies collectively demonstrate the ongoing efforts to enhance the efficiency and reliability of NVFFs, paving the way for their widespread adoption in energy-efficient systems.

With the pervasive use of portable electronic systems and IoT applications, the focus in designing IoT devices has shifted to prioritize lower energy consumption. This adjustment is crucial due to the prevalence of small batteries and methods like energy harvesting, leading to a substantial reduction in static and dynamic power—a formidable challenge [5, 6]. A pivotal component in digital VLSI is the flip-flop [7], facing scaling issues with transistors. Notably, static power consumption poses a significant concern [8]. Solutions like FLASH, resistive RAMs (ReRAMs), phase change memories (PCM), and spin transfer torque magnetic RAMs (STT-MRAM) have proven effective in mitigating static power [9,10]. These memory types store data before discontinuing the supply voltage and restore it upon reconnection, a state known as standby mode. In MRAM systems, the tunneling current's magnitude signifies the stored data as ZERO or ONE. MRAM, with its non-volatility, high speed, and ability for infinite cycling, stands as a near-perfect "universal memory" [11]. Among MRAM components, the SHE-MTJ device exhibits higher spin current injection efficiency than the common STT-MRAM devices, making it a more attractive choice [12]. Essentially, the Metal Tunnel Junction (MTJ) serves as the fundamental unit of Magnetic Random Access Memory (MRAM), comprising two ferromagnetic layers with an insulating layer in between. MTJ operation hinges on magnetization between the layers, leading to two major classifications: perpendicular MTJs, where magnetization is perpendicular to the film plane, and in-plane MTJs, where magnetization aligns parallel to the film plane.

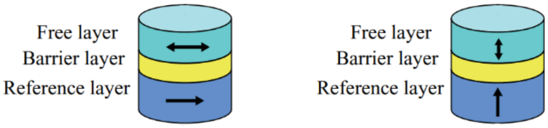


**Fig. 1.** MTJ magnetization [13]: a) In-plane b) Perpendicular

Perpendicular MTJs offer the potential for both thermal stability and reduced critical current density, boasting scalability to under 20 nm nodes—a notable advantage over In-plane MTJs. The academic and industrial focus is increasingly directed towards perpendicular Magnetic Tunnel Junctions (MTJs), recognizing their suitability for the next generation of logical and memory chips [13]. Consequently, our study incorporates perpendicular MTJs.

The design challenge lies in peripheral transistors crucial for providing the requisite current for efficient MTJ operation. Ensuring sufficient current necessitates wide peripheral transistors, introducing complications. Modern technologies like FinFET, replacing MOSFET transistors, enable the creation of more reliable and compact cells. FinFET allows adjustments to the transistor fin height, altering the channel width in the third dimension without affecting the device footprint. Compared to planar MOSFET, FinFET exhibits greater density and higher ON current with a smaller footprint. Despite requiring less space than MOSFET, FinFET demonstrates lower drain-induced barrier lowering, smaller subthreshold swing, higher ON/OFF current ratio, and lower threshold voltage roll-off. Additionally, FinFET's high gate control eliminates the primary source of threshold voltage variation in nanoscale CMOS transistors—random dopant fluctuation [11,14].

This study utilizes the master-slave flip-flop's basic design, rendering it non-volatile with efficiency by employing the SHE assisted MTJ device [11] and incorporating appropriately sized FinFET transistors from PTM [14]. The subsequent sections introduce MTJ and its variants, provide an overview of FinFET transistors, review previous works on non-volatile flip-flops and their structures, introduce our proposed nonvolatile flip-flop design, and present simulation results and analyses. The paper concludes with section 7.

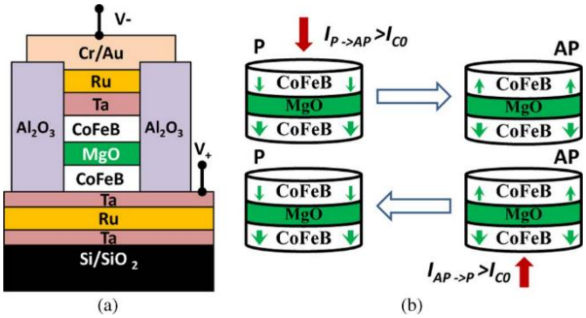


**Fig. 2.** a)Structure of an MTJ nanopillar b) STT write operation [15]

## 2. MTJ STRUCTURE

Spintronic circuit design utilizing magnetic tunnel junction (MTJ) devices has demonstrated encouraging outcomes. MTJ possesses certain distinct features such as high-speed access, non-volatility, extreme durability, and minuscule dimensions, making it an apt choice for logic chips and nonvolatile memories. Figure 2 illustrates that an MTJ consists of three layers, comprising two ferromagnetic layers separated by a thin oxide barrier sheet [15].One layer, called the pinned layer (PL), has a fixed magnetization while the other layer, called the free layer (FL), either has an anti-parallel (AP) or a parallel (P) magnetization that is not fixed. As a result, an MTJ device has two resistive states, high resistance (Rh or Rap) and low resistance (Rl or Rp) [8]. To switch the magnetization of the free layer, a charge current is passed through the MTJ device. The current becomes spin-polarized by the pinned layer and then exerts a spin torque to alter the magnetization of the free layer. This process is known as spin-transfer torque (STT) and serves as the typical write operation of MTJs. Despite its distinctive features, STT presents some concerns. One of them revolves around the heightened possibility of isolated layer breakdown, necessitating a reduction in the write current and consequently lengthening the write time. On the other hand, maintaining a high thermal stability ($\Delta$) while reducing switching current is a challenging task because $\Delta$ is proportional to I. This problem highlights the necessity for an alternative write operation for MTJ. One such device is the spin hall assisted MTJ which employs the Rashba and spin-Hall effect (SHE) and offers desirable properties such as lower energy consumption and faster operation compared to common STT devices.

The SHE assisted device is illustrated in Fig. 3. It is comprised of a three-terminal structure where a heavy metal strip is connected under the free layer of MTJ. In this device an In-plane charge current passes across the metal strip and by using the mentioned effects (SHE and Rashba) can produce a big enough spin torque to help with the STT current for changing the magnetization of free layer. It is worth mentioning that there are two kinds of writing operations and consequently designs, based on the magnetization anisotropy of MTJ devices i.e., i-MTJ and p-MTJ. The in-plane-anisotropy SHE MTJ (i-MTJ) is similar to the common STT switching with the difference being that the current passes through the heavy metal strip. This current can exert enough anti-damping torque to change the magnetization of the free layer.

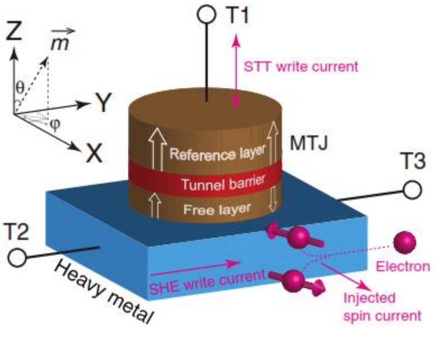


**Fig. 3.** Structure of SHE Asssisted MTJ [14]

The perpendicular-anisotropy SHE MTJ (p-MTJ), however, necessitates an additional magnetic field for the necessary charge current required for stable perpendicular magnetization. These write methods enhance the performance of the MTJ device for two reasons. The first being that by flowing current across the metal strip instead of the entire MTJ pillar, a high-speed read can be achieved without increasing the likelihood of insulated layer breakdown. Second reason for the low energy consumption during write operation is the high interaction of spin orbit in heavy metals and their low resistance, such as Ta with a resistance of approximately 190 cm. In memory systems, P-MTJs are more scalable due to their higher thermal stability compared to i-MTJs.

Tunnel magnetoresistance is among the major parameters of MTJ devices, essentially representing the difference between Rp and Rap. [8], [16]. The TMR ratio of MTJ nanopillars can reach up to 600% at room temperature, facilitating the detection of the state of MTJs by CMOS sense amplifiers [17].

$$TMR = \frac{Rap - Rp}{Rp} \times 100 \tag{1}$$

## 3. FINFET STRUCTURE

For many years, the primary focus in semiconductor devices has been on Bulk CMOS technologies. Moore's Law has encouraged scaling for performance enhancement features such as speed, space requirements, and power consumption. While scaling down circuits and systems can be advantageous, it also has certain drawbacks, such as higher sensitivity to process variations and short channel effects (SCE).

The application of bulk CMOS under 22nm has become unfeasible due to the short channel effects (SCE) which result in threshold voltage alteration, limitations in electron drift features, leakage current, and depletion of Ion/Ioff. The depletion of Ion/Ioff also leads to issues such as circuit design limitations in the subthreshold regime and reduced stability. Additionally, static power consumption increases with higher leakage current. Fig. 4 illustrates this phenomenon. FinFET technology has the potential to surpass the limitations of bulk CMOS transistors for sub 22nm scaling and can act as a valuable alternative to CMOS technologies.

The primary variance between bulk CMOS and FinFET transistors lies in the silicon fin, which functions as a channel for the flow of electron carriers between the source and the drain. Please refer to Figure 4 for clarity. The channel's gate section is surrounded from three dimensions, resulting in improved channel control. This depletion also prevents random dopant fluctuation (RDF), reducing sensitivity to process variations and lowering the occurrence of SCEs [18].

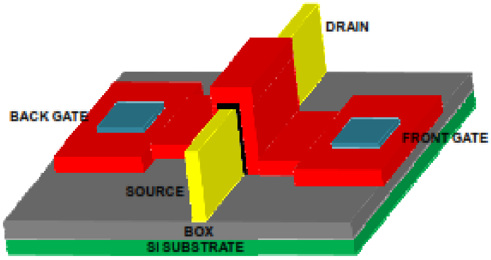


**Fig. 4.** Structure of FinFET [14]

## 4. PREVIOUS WORLS ON NONVOLATILE FLIP-FLOPS

Fig. 5 presents a comparison between the proposed nonvolatile flip-flop circuit and three others. In Fig. 5-a [19], a nonvolatile flip-flop of the master-slave type is displayed. However, it utilizes an in-plane MTJ device, which performs write operations solely with the SHE current that passes through strip metal. This highlights the requirement for wider transistors resulting in increased power consumption in contrast to SHE-assisted MTJs in the perpendicular category.

As shown in Figure 9c, a dual voltage nonvolatile flip-flop in [15] has been presented. This circuit employs SHE-assisted MTJ, similar to our proposed design, but includes a low-voltage master latch and a standard voltage non-volatile master latch. This technique results in significantly low power consumption. However, its implementation necessitates complex circuit design, an insertion of a supplementary voltage converter circuit, and a requirement of two independent voltage sources. Furthermore, the additional converter circuit employs a high number of fins, and the use of dual transistor technologies further complicates production. In [20], two non-volatile flip flops are presented in Fig. 9-a. The first circuit has a similar overall structure to the one introduced in [19], but by removing the feedback loop's transmission gate from the write operation path, the resistance of the route is reduced, as well as the size of the write transistors. Nevertheless, it still employs the same MTJ technology as [19], demanding high switching current and consequently high energy consumption.

The second nonvolatile flip-flop introduced in [20] (Fig. 9-b) uses the same MTJ technology as the first circuit but achieves lower current and energy consumption by employing a series arrangement of MTJ devices. However, the use of in-plane SHE MTJ technology still results in overall high write energy consumption. In contrast to most non-volatile flip-flops, the non-volatile feature is designed on the master latch. Furthermore, a SHE-assisted MTJ is used for superior performance and power consumption. Also, the transmission gate between the inverters is eliminated in favor of lower resistance on the write path.

Figure 5-b [8] portrays a master-slave D flip-flop. Figure 5-c depicts another non-volatile D flip-flop circuit. The design differs from its predecessor in terms of the number of transistors employed in the write and read paths, leading to a lower transistor count for the MTJ operation depicted in Figure 5c. Previous flip flops, presented in references [8] and [19], utilized the current that flowed through the transistors of inverters for the write path, where overall wide transistors were required to supply the write current to two MTJ devices.

**Table 1**. Critical MTJ Parameters

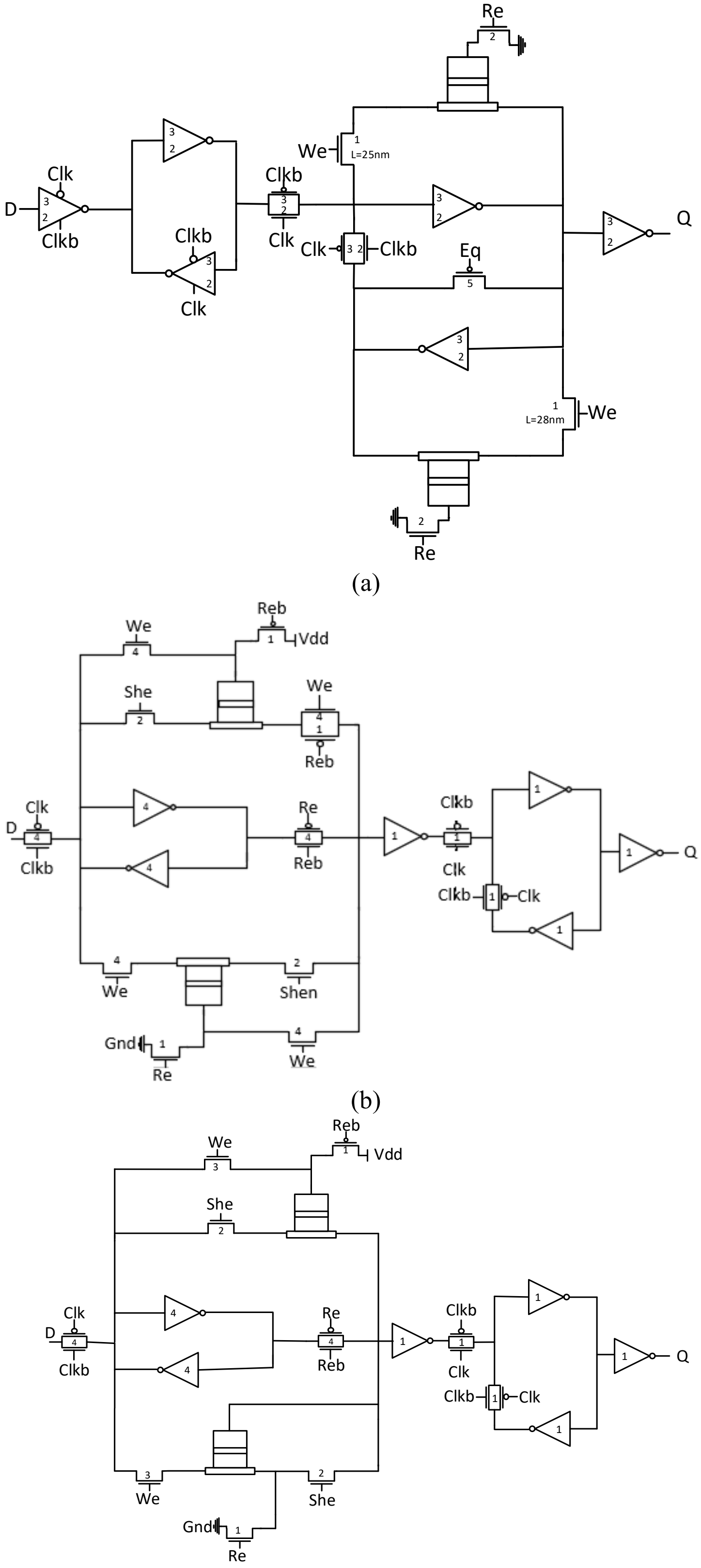
| *Parameter* | *Value* |
|---|---|
| D (diameter) *(nm)* | 50 |
| Tox (mgo barrier thickness) *(nm)* | 1.1 |
| Tsl (Free layer thickness) *(nm)* | 0.7 |
| Metal strip dimensions(l,d,w) *(nm)* | (3,20,20) |
| TMR | 250% |

**Table 2**. Critical FinFET Parameters

| *Parameter* | *Value(nm)* |
|---|---|
| Gate Length (L) | 11 |
| Fin Height (Hfin) | 18 |
| Equivalent Oxide Thickness (EOT) | 0.62 |
| Fin Pitch (Pfin) | 22 |
| Fin Thickness (Tfin) | 6.5 |

**Table 3**. Transistor Sizings

| *Transistors* | *Fin number* |
|---|---|
| Master latch inverters,tg0 & tg1 | 3 |
| Inv 2 and slave latch transistors | 1 |
| Peripheral We transistors | 4 |
| She transistor | 3 |
| Main Read transistors | 1 |
| Middle We transistor | 3 |



(a)

(b)

(c)

**Fig. 5.** Some of the compared Nonvolatile Flip-flops a) SHE-NVFF [15] b) Sym-NVDFF [8] c) Asym-NVDFF [8]

## 5. PROPOSED SHE-ASSISTED NONVOLATILE FLIP-FLOP

The proposed design is depicted in Fig. 6. The slave latch of the flip flop is based on the common design. The design is based on the flip flops of [8].

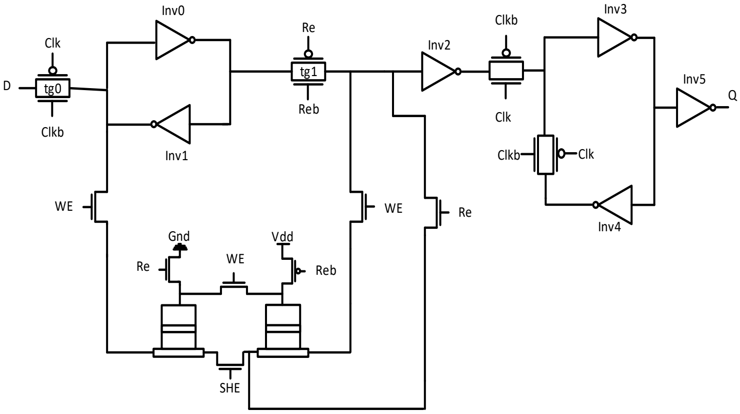


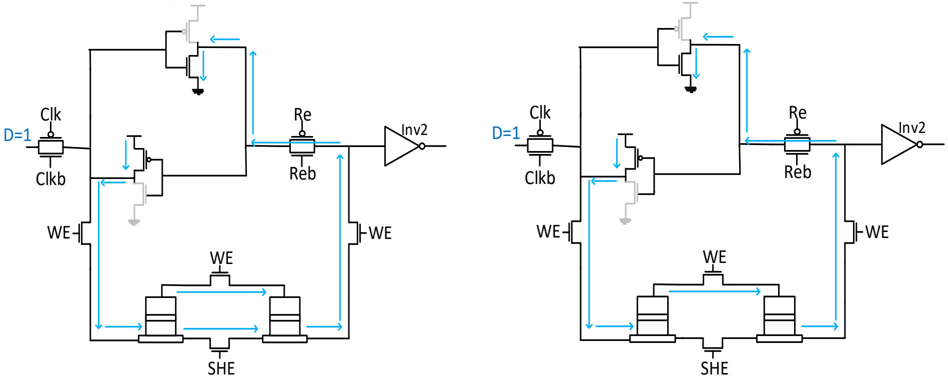
**Fig. 6.** Proposed design

### 5.1. Normal operation

In this mode, the circuit functions as a standard D flip-flop. When the clock is low, the input data proceeds through the master latch and, upon clock rising, is stored in the master loop, then transmitted through the slave latch and into the flip-flop's output. When the clock is low, the input data proceeds through the master latch and, upon clock rising, is stored in the master loop, then transmitted through the slave latch and into the flip-flop's output. Subsequently, when the clock drops again, the output data is stored within the slave latch's feedback loop as the input data proceeds once more through the master latch.

### 5.2. Write operation

This process is executed prior to cutting off the Vdd, while maintaining a high clock to avoid interference during storage in MTJ. As illustrated in Figure 7, depending on the data, either inv1 or inv0 will provide a complementary value. Thus, if the data is 1, the NFET of Inv 0 and the PFET of Inv1 will activate, generating a current that flows from the PFET to the NFET. These MTJ devices are situated along this current's path. The SHE transistor remains active for 400ps to enable the passage of current through the strip metals and facilitate the write operation. The peripheral transistors of MTJ are adjusted to ensure sufficient current for the write operation. Upon completion of the write operation, one of the MTJ devices will have a parallel configuration while the other will have an anti-parallel configuration resulting in different resistances in accordance with the stored data.



(a) (b)

**Fig. 7.** Two levels of write operation a) SHE and STT drive current through MTJ b) SHE is turned off and current is driven only by WE signal

### 5.3. Read operation

In this operation, as depicted in Figure 8, the RE signal is raised and the path to the master latch inverters is cut off to avoid any disturbance during reading. Unlike the flip flops, which have a non-volatile slave latch that requires the clock to be low in order to read the data into the output, in this circuit, the read operation should be performed while the clock is still high to transfer the stored data to the flip flop's output. The reading should be carried out just before the clock goes down. During the reading process, read transistors and a single she transistor are activated to provide a pathway for a small current to pass through two MTJ devices from Vdd to ground. Depending on the resistance of the MTJ devices, the voltage between them may be higher or lower than half of Vdd. A pathway is then established from this point to the input of inv2, enabling the data to be restored to the flip flop. Technical abbreviations will be explained as they are used.

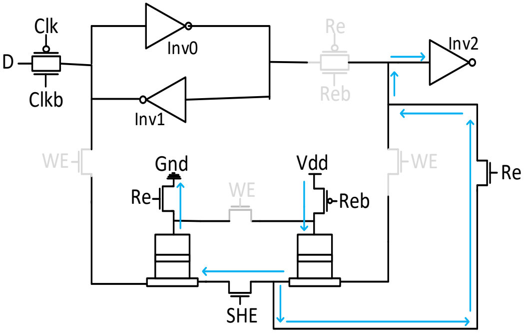


**Fig. 8.** Read operation

## 6. RESULTS AND COMPARISON

The designs were simulated using Hspice software and PTM [14] transistor models with a nominal voltage of 0.7v on 7nm FinFET technology. The simulations were set to a length of 11nm, except for circuit [19] depicted in Fig. 5 (a) which utilized a higher length proportional to the original length value for two transistors. The number of fins employed in each design is illustrated in Fig. 5 and Fig. 6. The utilized MTJ parameters are derived from the original values detailed in papers [8],[15],[19], which mainly cover CMOS technology nodes. In adapting to FinFET technology, some adjustments in sizing were necessary to obtain optimal performance. The MTJ model utilized for the proposed design is referenced from [21]. Table 4 depicts the simulation results obtained from comparing the proposed flip-flop against other counterparts. The operation of the proposed design is illustrated in Fig. 10. The flip flop operates within normal parameters from 0 to 25ns, following which the clock rises. Subsequently, the write signal begins after 0.5ns at 25.5 ns, and both the write and she signals are turned on and held for 400 ps. This results in a change in the magnetization of MTJ devices: Mz0 goes anti-parallel (high resistance) while Mz1 goes parallel (low resistance). Shortly after, VDD is turned off. After applying VDD, the read signal activates for 2ns along with a raised clock and she signal. Based on the state of MTJ devices and the resulting low voltage between them, the PFET of inv2 turns on and restores an output of 1 to the circuit.

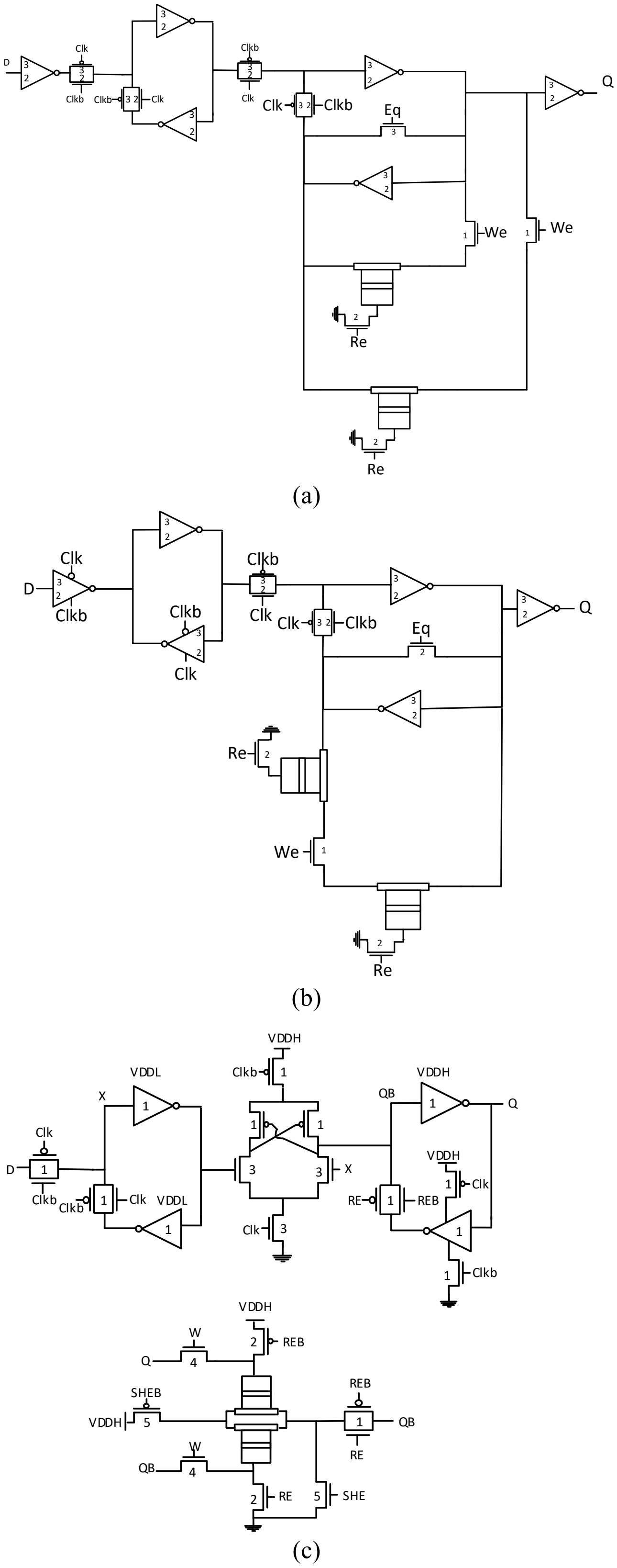


**Fig. 9.** Some of the other compared Nonvolatile Flip-flops a) pSOT-NVFF[20] b) sSOT-NVFF[20] c) NVLCFF[15]

The compared parameters are stated in Table 4. Dynamic power is the power consumed during switching of output from 0 to 1 and from 1 to 0 and PDP is resulted from multiply of normal operation average power to clk-q delay. As it can be seen in Table 4 NVLCFF has the highest clk-q delay and proposed design has the lowest by 5%. Write energy of both NVLCFF and proposed design are lower than other circuits, however the proposed design wins over NVLCFF by over 5 times of improvement.

The proposed design shows a 17% improvement in PDP. The lowest read energy consumption is shared between NVLCFF and the proposed design, with NVLCFF exhibiting an exceptionally low consumption rate. SHE-NVFF has the highest energy consumption in both write and read energy. The read signal time was equal for all simulations. The highest static power consumption is exhibited by pSOT-NVFF and Asym-NVDFF. Apart from NVLCFF, which consumes the least static power, the proposed design has a static power consumption more than 19% lower than the other circuits. SHE-NVFF and pSOT-NVFF demonstrate the highest dynamic power consumption, while the proposed design, along with Asym-NVDFF and Sym-NVDFF, exhibit the lowest dynamic power. However, in terms of PDP, Asym-NVDFF has the highest, and the proposed design has the lowest.

Both NVLCFF and the proposed design exhibit the lowest average power consumption. Although the write delay of the proposed design, along with Asym-NVDFF are the most significant, the proposed design surpasses in PDP, write energy and clk-q delay. Generally, NVLCFF excels in most other areas, but by consuming the least static power and read energy, it has the highest clk-q delay and consequently the highest PDP. This makes the proposed design the best overall circuit by having the lowest write energy and PDP.

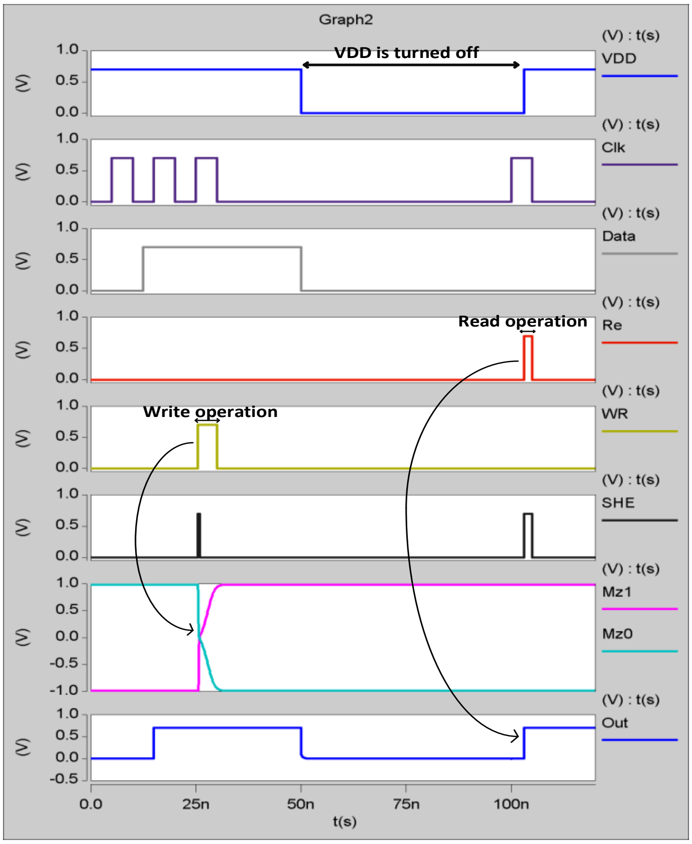


**Fig. 10.** Operation of the proposed flip-flop

**Table 4**. Results of comparisons between the proposed flip- flop and similar flip-flops

| | **MTJ Device** | **Clk-q delay (ps)** | **Write delay (ns)** | **Write energy (fj)** | **Read energy (fj)** | **Static power (nw)** | **Dynamic power (nw)** | **Average power (nw)** | **PDP (aj)** |
|---|---|---|---|---|---|---|---|---|---|
| She-NVFF[19] | SHE MTJ | 5.5 | 1.9 | 212.3 | 93.4 | 53.2 | 214.6 | 112.8 | 0.62 |
| Sym-NVDFF[8] | SHE assisted STT MTJ | 5.3 | 5.9 | 119.8 | 15 | 38.7 | 74.4 | 143 | 0.75 |
| Asym-NVDFF[8] | SHE assisted STT MTJ | 5.2 | 7 | 108.8 | 13.8 | 58.3 | 86.5 | 155.1 | 0.81 |
| NVLCFF[15] | SHE assisted STT MTJ | 19.3 | 6.9 | 44.5 | 0.4 | 17.8 | 107.2 | 41.1 | 0.79 |
| pSOT-NVFF[20] | SHE MTJ | 5.7 | 4.6 | 247.3 | 29.3 | 61.5 | 214.6 | 124.8 | 0.72 |
| sSOT-NVFF[20] | SHE MTJ | 5.3 | 3.4 | 135.9 | 29.2 | 55.5 | 210.9 | 118.1 | 0.63 |
| Proposed design | SHE assisted STT MTJ | 4.9 | 7 | 20.3 | 4.1 | 31.1 | 74.6 | 105.6 | 0.51 |

## 7. CONCLUSION

In this study, we introduce a master-slave flip-flop by combining MTJ structures and FinFET transistors, resulting in lower write energy consumption compared to equivalent circuits. The series implementation of SHE-assisted MTJ devices reduces the required current for changing the MTJ states and leads to smaller transistor sizes, resulting in reduced power and energy consumption in the flip-flop circuit. The proposed circuit exhibits strong performance in read energy, static power, and dynamic power. Furthermore, it outperforms other circuits by up to 5-54%, 54-91%, and 17-37% in parameters such as clk-q delay, write energy and PDP. These findings demonstrate the efficacy of the proposed design.

## CONFLICTS OF INTEREST

The authors declare no conflict of interest.

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