

# An overview of FPGA-based digital insulin-glucose implementations Regulator for type 2 diabetic patients

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| ARTICLE INFO   | ABSTRACT  |
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| <p>Article History:<br/>Received 2 April 2024<br/>Received in revised form 28 May 2024<br/>Accepted 12 June 2024<br/>Available online 20 June 2024</p> | <p>This study details the development of a digital insulin-glucose regulation system for type 2 diabetes management, utilizing a Field Programmable Gate Array (FPGA) board. The system is designed to monitor and control insulin levels in patients by measuring their blood glucose levels only. Unlike other solutions that rely on general-purpose programmable hardware, this regulator is built entirely on a hardware-based architecture without the need for software, as elaborated in this document. A prototype was created to test its effectiveness in two scenarios: (i) an open loop mode where the regulator operates independently, and (ii) a closed loop mode where it functions as an artificial pancreas and is linked to a group of one hundred virtual patients. These patients were created using a detailed theoretical model approved by the U.S. Food and Drug Administration for pre-clinical trials of glucose regulation methods. The virtual patients exhibit similar patterns in glucose fluctuations with varying peak and trough levels post-meal. The outcomes of these tests are analyzed and compared with results derived from theoretical model simulations conducted in SIMULINK. The comparison shows relative errors within <math>\pm 1\%</math>, indicating the high precision of this digital insulin-glucose regulation system. The hardware implementation processes each virtual patient's glucose data in approximately <math>1.1 \mu\text{s}</math> and consumes about <math>36 \text{ mW}</math> of power. These promising results encourage further research into digital systems for glucose regulation that could be incorporated into very-large-scale integration (VLSI) as System-on-Chips or Lab-on-Chips. Such developments could pave the way for advanced, miniaturized devices suitable for portable, wearable, and implantable medical applications.</p> |
| <p>Keywords:<br/>Digital Architectures, Digital Controllers, Diabetes Mellitus, Type-2 diabetes, FPGA, Insulin-Glucose Regulators, VLSI</p>            |   |

## 1. INTRODUCTION

Diabetes Mellitus (DM) is a long-term medical condition where the hormone insulin fails to adequately regulate blood glucose levels. There are two primary forms of this disease: Type 1 Diabetes Mellitus (T1DM), characterized by the pancreas's complete inability to produce insulin, and Type 2 Diabetes Mellitus (T2DM), where the body

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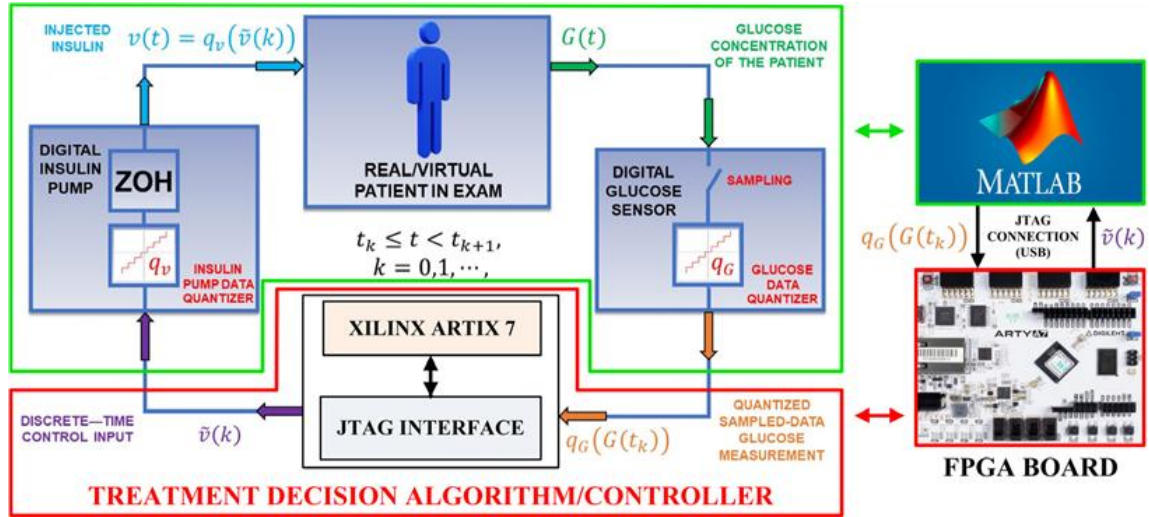
cannot sufficiently adjust blood glucose levels due to inadequate insulin production and often, insulin resistance. T2DM is more prevalent, affecting over 415 million individuals globally and significantly impacting national healthcare budgets. Recent findings indicate that SARS-CoV-2 infections have notably increased insulin requirements. For managing T1DM, various Artificial Pancreas (AP) systems have been developed to regulate blood glucose and thus improve the quality of life for patients. However, there are relatively few similar innovations available for T2DM in existing literature. Technically, AP systems integrate sensors, actuators, and control mechanisms to administer glucose regulation therapy, taking into account the patient's daily lifestyle needs. An essential element in developing a glucose regulator for an Artificial Pancreas (AP) involves considering the frequency at which patient glucose levels are sampled and how these measurements are digitized in electronic devices. Researchers have suggested glucose regulators that utilize both insulin and glucose data for Type 2 Diabetes Mellitus (T2DM) patients. However, in real-time AP functions, direct insulin monitoring is impractical due to the necessity for specific chemical reagents, a limitation that can be circumvented by focusing on blood glucose level measurements. Consequently, there has been significant emphasis on the hardware design of glucose regulators to create control systems suitable for portable and wearable devices that operate under low-voltage and low-power conditions, enhancing reliability, safety, and affordability.

Investigations into embedded solutions using microcontrollers, including smartphone integration, have been conducted. Such control systems can monitor glucose levels and appropriately manage insulin infusion via pumps, ensuring the medical device's hardware security. These systems typically rely on commercially available programmable hardware components, which do not support the integration of analog and digital circuits on-chip a strategy essential for reducing system size, weight, and power consumption. To address this issue, Field Programmable Gate Array (FPGA)-based approaches are widely adopted for rapid prototyping and testing of bespoke integrated solutions and managing digital system communications in biomedical applications.

The theoretical model of a digital static output feedback glucose regulator that accounts for quantization in both input and output channels was outlined. Building on this model, this paper introduces a complete hardware implementation of a quantized sampled-data glucose regulator on an FPGA board specifically for T2DM patients. Unlike previous studies, this paper provides an exhaustive description of the digital architecture implemented and includes a series of measurements to validate the performance of the insulin-glucose regulator across a cohort of one hundred different Virtual Patients (VPs), utilizing a theoretical model approved by the U.S. Food and Drug Administration for pre-clinical validation of glucose control strategies. The experimental findings confirm that the control of insulin levels in the patient's body deviates by only 1% from theoretical expectations, with a total power consumption of 36 mW. These results underscore the efficacy of the proposed solution in terms of medical response accuracy and energy efficiency. Furthermore, the FPGA-based design paves the way for developing a microelectronic integrated System-on-Chip for the insulin-glucose regulator, enabling fully-hardware operation without reliance on software. [1-17]

## **2. VIRTUAL CLINICAL ENVIRONMENT**

Figure 1 illustrates the comprehensive closed-loop control system of the glucose regulator designed for pre-clinical testing. Focusing initially on the left section of Figure 1, the upper box framed in green depicts the virtual patient (VP) body. This box simulates the VP's physiological reactions to changes in glucose and insulin levels through differential equations. Below this, in a red frame, lies the insulin treatment decision controller, which is part of the artificial pancreas (AP) system. This controller functions based on the algorithm detailed. It is crucial to acknowledge that the design shown in Figure 1 also facilitates the evaluation of various mathematical models for glucose-insulin regulation systems. These models incorporate a meal simulation model tailored specifically for such frameworks. Additionally, this design has proven highly effective in accurately addressing the clinical requirements of Type 2 Diabetes Mellitus (T2DM) patients. It forms the foundation of the UVA/Padova Type 1 Diabetes Simulator, which is endorsed by the U.S. FDA as a viable substitute for animal testing and is widely referenced in AP research literature.



**Fig. 1.** To the left, there is a depiction of the closed-loop control configuration for the insulin-glucose regulator. To the right, one can see the SIMULINK model that simulates the Virtual Patient (VP) alongside the FPGA board that executes the Artificial Pancreas (AP) system. [37]

As illustrated in the left section of Figure 1, the insulin-glucose regulation system is composed of two primary components: the Virtual Pancreas (VP), represented by the green-outlined upper box, and the treatment decision controller, shown in the red-outlined lower box, which emulates the functionalities of an Artificial Pancreas (AP). These components form a closed-loop control system.

The system functions as follows:

1. At each discrete time instant  $t_k$ , the VP generates a glucose concentration signal  $G(t)$ , which is sensed by a digital glucose sensor. This sensor quantizes the signal into digital values  $q_G G(t_k)$ , emulating the analog-to-digital conversion process at each sampling point.
2. These quantized readings are used as input to the treatment decision controller. To refine the glucose estimate, the controller also uses buffered data from the previous sampling instant  $t_{k-1}$ , producing an interpolated value of the form  $q_G[\alpha G(t_{k-1}) + (1-\alpha)G(t_k)]$ , where  $0 \leq \alpha \leq 1$  is a tunable parameter reflecting the dynamic interplay between glucose and insulin in the VP.
3. Based on this interpolated glucose estimate, the controller computes the corresponding digital insulin concentration.
4. This insulin value is then processed by a digital insulin pump, which transforms it into a quantized signal  $q_v v(k)$ , where  $q_v$  denotes a constant related to the pump's operating characteristics (e.g., the number of pulses required to deliver a specified insulin dose).

Since insulin infusion can occur continuously between two sampling points  $t_k$  and  $t_{k+1}$ , the insulin delivery over this interval is modeled as  $v(t) = q_v v(k)$ .

The closed-loop architecture has been implemented through two distinct approaches:

- **Software-only implementation:** Both the VP and AP modules (green and red boxes in Figure 1) are modeled entirely in SIMULINK. Here, all signal computations including  $q_G G(t_k)$ ,  $v(k)$ , and  $v(t)$  are generated within the software environment. These results are referred to as *software data*.
- **Software/hardware co-design:** As shown on the right side of Figure 1, while the VP continues to be simulated using the SIMULINK model, the treatment decision controller is implemented on a Xilinx Artix-7 FPGA. In this setup, insulin concentrations are computed on the FPGA, and these outputs are referred to as *hardware data*.

In both implementations, glucose levels from the VP are recorded every 10 minutes over a 24-hour simulation period, and corresponding insulin doses are determined.

In the hardware-based architecture, a MATLAB R2022a script reads each quantized glucose value  $q_G G(t_k)$  from the SIMULINK model and converts it into a 32-bit single-precision floating-point number. This value is then written to a dedicated RAM block on the FPGA via a JTAG interface. After the treatment decision controller processes the data and computes the optimal insulin concentration  $v(k)$ , this result is also written back into the same RAM block. The SIMULINK model then retrieves  $v(k)$ , enabling the digital insulin pump to deliver the corresponding insulin dose  $q_v v(k)$  to the VP before the next glucose reading is taken.

Figure 2 provides a detailed view of the digital architecture of the FPGA-based controller, and the associated schematic diagram is shown in Figure 3.

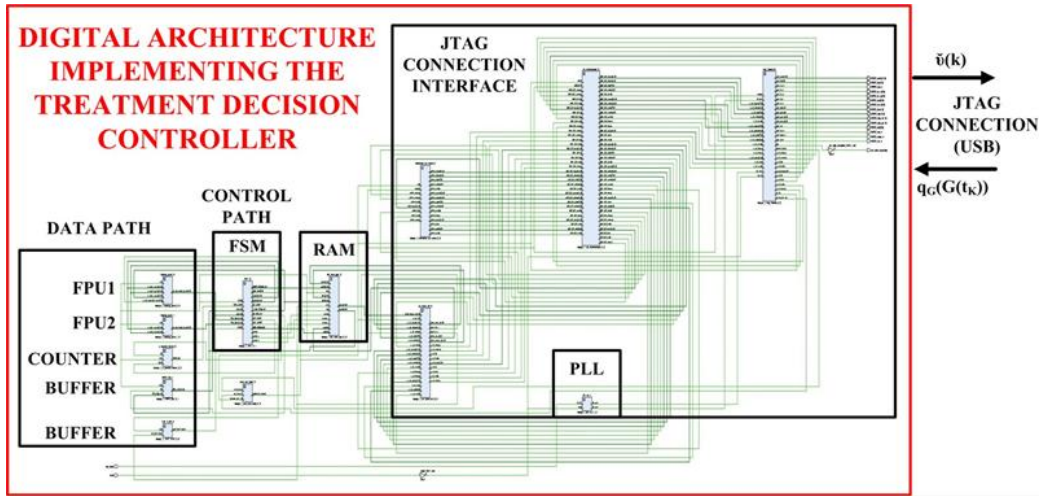


Fig. 2. Digital architecture implementing the insulin treatment decision controller on the FPGA board. [37]

Referring to Figure 1, Figure 2 illustrates the comprehensive digital system deployed on the XILINX ARTIX 7 FPGA-based board. This system includes a JTAG connection interface that facilitates data transmission to and from the VP, along with a processing unit designed to manage the insulin treatment decision controller. In more detail, operations within the system are executed by the DATA PATH block, which features an Arithmetic Logic Unit (ALU) consisting of two Floating Point Unit (FPU) modules, namely FP1 and FP2, a COUNTER module, and two data BUFFER modules. The FPU1 module is responsible for performing Multiply-Accumulate (MAC) and subtraction operations, while the FPU2 module handles division operations. The COUNTER module functions as a timer, and the two BUFFER modules are utilized for storing intermediate results of operations. The CONTROL PATH block includes a Finite State Machine (FSM) module, based on the Moore model, which orchestrates the algorithmic operations. The RAM block retains the initial glucose and insulin concentration values along with the outcomes of completed processes as previously mentioned. Additionally, a Phase-Locked Loop (PLL) block generates the machine clock CLKM, and the INTERFACE CONTROLLER block oversees communications between the FPGA board and the VP body.

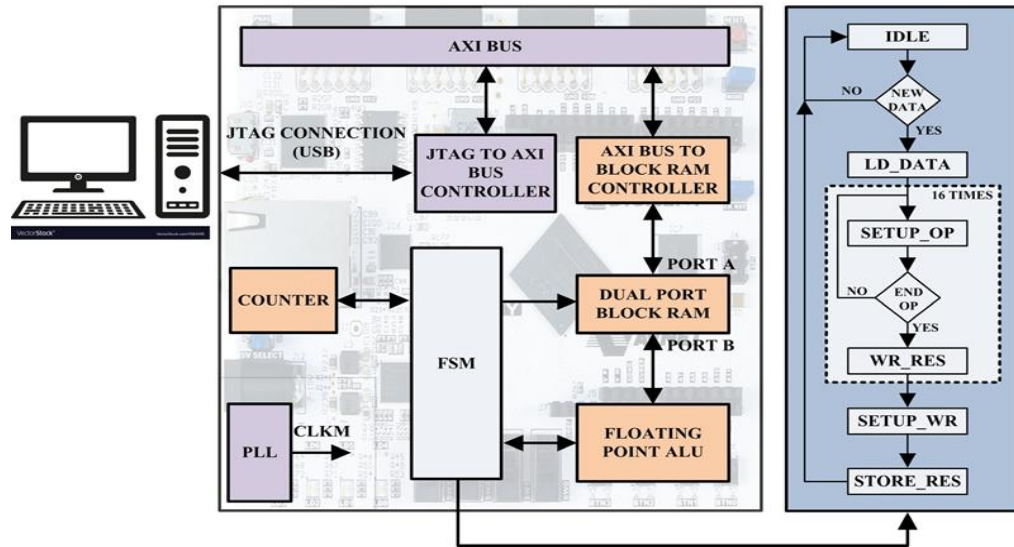


Fig. 3. Digital architecture at block level of the insulin treatment decision controller implemented on the FPGA board. [37]

In the left portion of Figure 3, the block diagram of the treatment decision controller illustrates the management of input/output data via the AXI BUS CONTROLLER module. This data is transferred through the AXI BUS interface and subsequently written to or read from a true dual-port block RAM using the BLOCK RAM CONTROLLER. At each sampling instance  $t_k$ , a new glucose concentration value is stored in memory. The Finite State Machine (FSM) module then accesses this value to orchestrate the sequence of control operations, which are executed by the DATA PATH module described earlier in Figure 2.

Following the computation of the insulin concentration, the FSM writes the resulting data back into the dual-port block RAM. This value is then retrieved by a MATLAB script and transmitted to the SIMULINK model, where it is used to initiate insulin delivery into the virtual patient (VP). A Phase-Locked Loop (PLL) module generates a clock synchronization signal, CLKM, operating at 166 MHz to coordinate timing across the digital system.

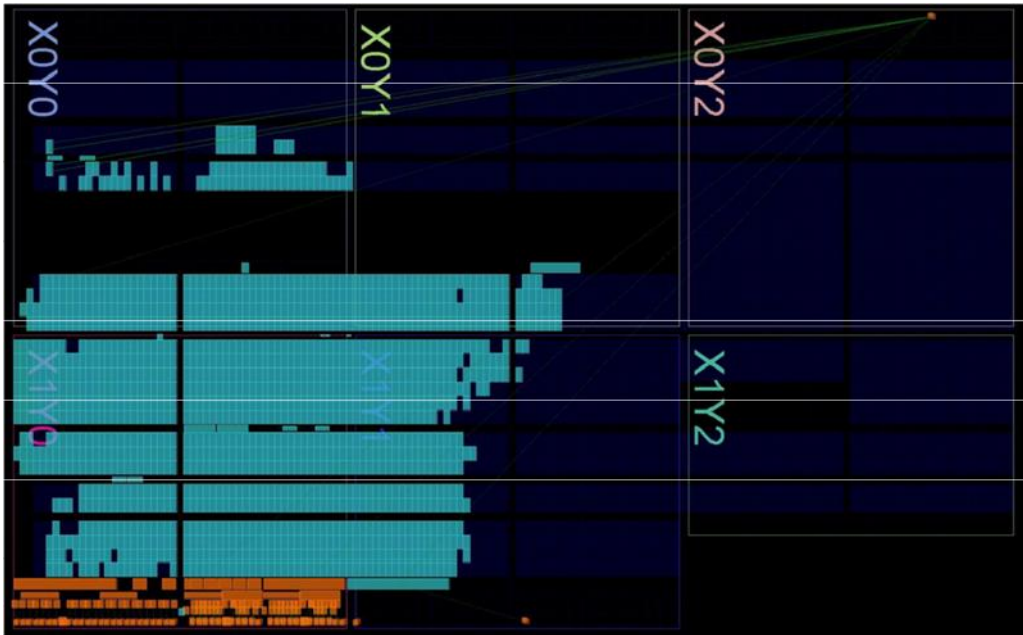
In the right section of Figure 3, the FSM module architecture is detailed. It consists of 36 distinct states, including 32 operational states, 3 initialization/setup states, and 1 idle state. The FSM control flow follows a structured process:

1. The system remains in the IDLE state until new data is flagged as ready.
2. Upon detection, the FSM fetches the marked data.
3. It then configures the inputs of the floating-point arithmetic logic unit (ALU) to execute the 16 predefined instructions.
4. The FSM identifies the specific operations to be performed.
5. After computation, it waits for the results generated by the DATA PATH module.
6. Finally, the FSM stores the output in a designated address within the BLOCK RAM.

Figure 4 presents the overall digital system architecture supporting insulin treatment decision-making, implemented on a Xilinx Artix-7 FPGA board. Resource utilization for this system is detailed in Table 1. As indicated in Figures 2 and 4, the system architecture is designed to encompass both the treatment decision controller and its interface with the VP, facilitating testing and validation processes.

The hardware controller alone occupies approximately 5% of the FPGA's total resources, specifically utilizing 1,663 Look-Up Tables (LUTs), 2,575 Flip-Flops (FFs), two 18-kb block RAMs (RAMB18E1), and four DSP48E1 multiply-accumulate (MAC) units. This configuration supports the execution of glucose data processing tasks within

1.122 microseconds. The dynamic power consumption associated with the operation of the insulin treatment decision controller is estimated to be 36 mW.

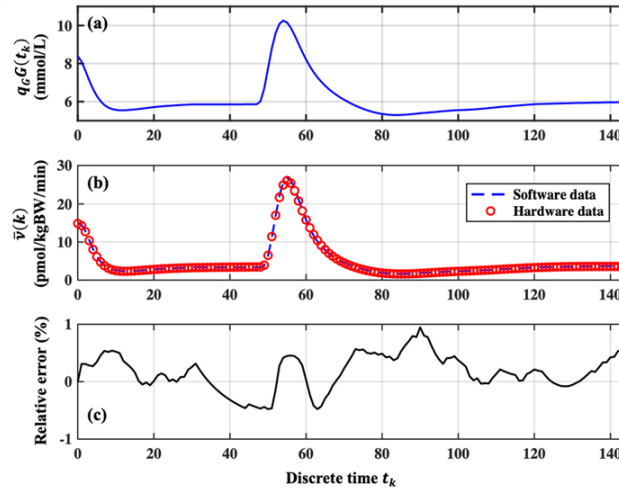


**Fig. 4.** Floorplan of the complete digital system implemented on the commercial XILINX ARTIX 7 FPGA-based board. [37]

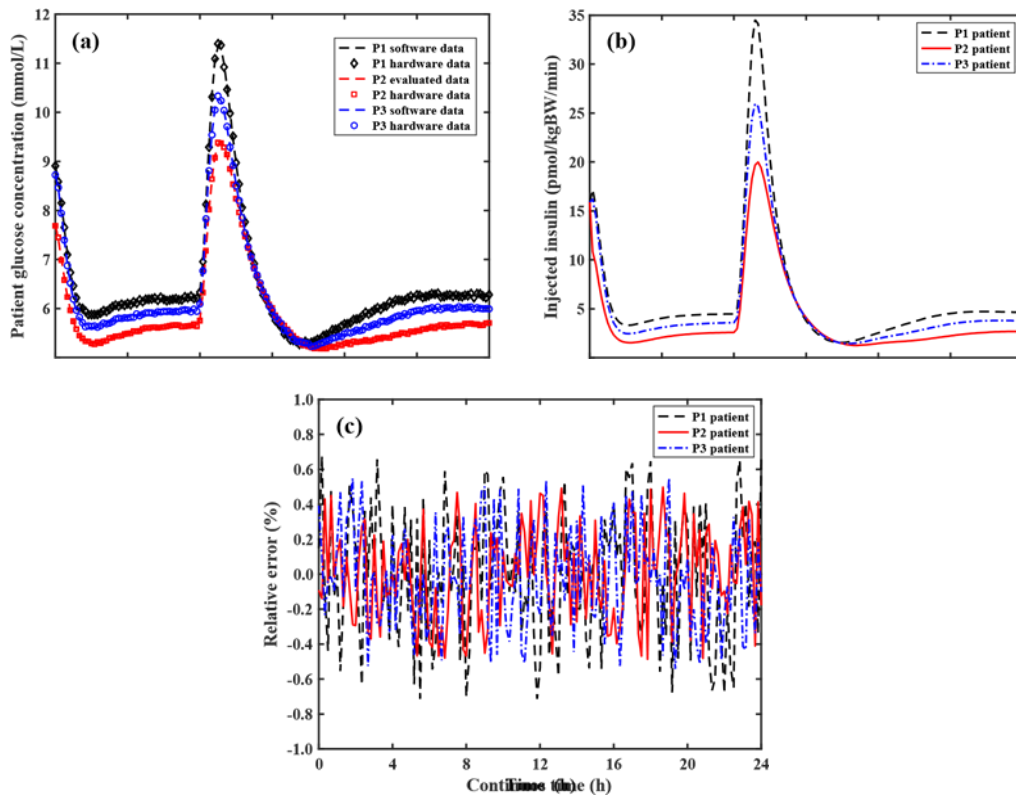
**Table 1.** Used resources by the complete digital system implemented on the commercial XILINX ARTIX 7 FPGA-based board. [37]

|                        | <b>Implemented System</b> |      |
|------------------------|---------------------------|------|
| <b>Slice LUTs</b>      |                           | 7924 |
| <b>Slice Registers</b> |                           | 8598 |
| <b>F7 Muxes</b>        |                           | 102  |
| <b>F8 Muxes</b>        |                           | 1    |
| <b>Slice</b>           |                           | 2670 |
| <b>LUT as Logic</b>    |                           | 7138 |
| <b>LUT as Memory</b>   |                           | 786  |
| <b>Block Ram Tile</b>  |                           | 2    |
| <b>DSPs</b>            |                           | 4    |

Figure 5. Insulin-glucose regulator function in open loop conditions and Figure 6, It shows the function of the insulin-glucose regulatory system in closed loop conditions.



**Fig. 5.** Operation of the insulin-glucose regulator under open loop condition. Panel (a): Example of the variation of the VP glucose concentration in 144 steps taken every 10 min; Panel (b) Comparison between the software and hardware data achieved by emulating the treatment decision controller by the SIMULINK model and implemented by the FPGA board; Panel (c) the point-by-point relative errors between the two set of data reported in Panel (b). [37]



**Fig. 4.** Operation of the insulin-glucose regulator system under the close loop condition. Panel (a): Variation of the software and hardware data of the glucose concentration for the three VPs during a day; Panel (b): Insulin concentration infused in the VP bodies determined by the treatment decision controller implemented by the FPGA board; Panel (c) Point-by-point relative error between the software and hardware data of Panel (a). [37]

### 3. CONCLUSION

The manuscript elaborates on the deployment of a Xilinx Artix 7 FPGA board to manage an insulin-glucose regulation system for individuals with type 2 diabetes, which functions by solely monitoring blood glucose levels. The entire framework outlined in the theoretical model approved by the U.S. Food and Drug Administration for pre-clinical trials of glucose regulation methods has been adapted and executed on the FPGA board, with appropriate processing by the designed hardware structure. This leads to an entirely hardware-based operation of the insulin-glucose regulator, establishing a foundation for the specialized creation of microelectronic architectures intended to supplant the general-purpose programmable hardware typically used in comparable existing systems.

The prototype created was tested to assess the effectiveness of the proposed architecture under both open-loop scenarios, where only the insulin-glucose controller is active, and closed-loop scenarios, where the controller serves as an artificial pancreas for virtual patients modeled in SIMULINK. The system's validation involved using a clinical sample of one hundred virtual patients who exhibit similar daily fluctuations in glucose levels with varying peaks and troughs during meal times. Performance evaluations of the insulin-glucose regulator in closed-loop conditions utilized the aforementioned theoretical model in SIMULINK to emulate virtual patients linked to the controller on the FPGA board. Experimental outcomes in both open-loop and closed-loop scenarios indicated a relative error of less than  $\pm 1\%$  compared to predictions from the theoretical model. The regulator processes input data on glucose concentrations from virtual patients and calculates the required insulin doses to be administered within approximately  $1.1 \mu\text{s}$ , while maintaining total power consumption around  $36 \text{ mW}$ . Efforts are currently underway to reduce power consumption, size, and overcome existing limitations and complexities associated with using an FPGA board by developing an integrated microelectronic System-on-Chip (or Lab-on-Chip) for the proposed system. This advancement is crucial for implementing a fully-hardware integrated solution in portable, wearable, and implantable biomedical applications.

### **Declaration**

We acknowledge that we used ChatGPT to enhance the academic writing of our manuscript while ensuring the originality and integrity of our work.

### **Transparency Statement**

The data supporting this study are available upon reasonable request to the corresponding author, subject to ethical and confidentiality considerations.

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### **Declaration of Interest**

The authors declare that they have no competing interests.

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