Transactions on Machine Intelligence 7(4) (2024) 286-295

ISSN Online: 2821-1693

Transactions on Machine Intelligence

Journal Homepage: https://tmachineintelligence.ir/index.php/TMI

A Novel Frequency Compensation Scheme for Stabilizing Three-Stage Amplifiers for a Wide range of Load Capacitors

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ARTICLE INFO

Article History:
Received 2 August 2024
Received in revised form 29 September 2024
Accepted 22 December 2024
Available online 27 December 2024

Keywords:
Operational Transconductance Amplifier (OTA), Three-Stage Amplifier, Wide Load Capacitors.

ABSTRACT

This paper introduces an innovative frequency compensation method designed to enhance the stability of three-stage amplifiers without imposing limitations on capacitive loads (CL). Traditional multistage amplifiers often encounter stability challenges due to varying CLs, but the proposed scheme overcomes this issue through an advanced compensation strategy. The approach integrates Miller capacitors in series with embedded current buffers and incorporates a feedback network connecting the second stage to the first. By effectively tuning the quality factor of non-dominant poles, the method achieves robust stability across a broad range of capacitive loads. The design was implemented using standard 180 nm CMOS technology, operating at a nominal supply voltage of 1.8 V. The compact layout occupies only 0.0026 mm² and consumes 23.38 µA of current. Open-loop frequency response simulations across different CL values, ranging from 0 to 100 nF, demonstrated a high gain of 119.3 dB. The average unity-gain bandwidths were measured at 4.872 MHz, 2.4 MHz, and 90.11 kHz for no load, 0.1 nF, and 100 nF loads, respectively. The paper also evaluates the amplifier's output settling performance under varying load conditions. Configured as a buffer with a 0.4 V input step, the amplifier exhibited stable behavior across all tested CLs. The measured 1% settling times were 0.48 µs for a 100 pF load and 19.92 µs for a 100 nF load, highlighting the effectiveness of the proposed compensation scheme in ensuring stability and performance for three-stage amplifiers.

1. INTRODUCTION

In the realm of electronic circuit design, amplifiers play a pivotal role in enhancing the power of a signal [1]. Among various types of amplifiers, the three-stage amplifier has gained significant attention due to its ability to provide high gain and bandwidth. However, designing a stable three-stage amplifier that can handle a wide range of load capacitors remains a challenging task. The stability of an amplifier is a critical aspect that determines its performance and reliability. Instabilities can lead to undesirable oscillations, degrading the quality of the amplified signal and potentially damaging the amplifier. Therefore, ensuring stability is a paramount concern in amplifier

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http://dx.doi.org/10.47176/TMI.2024.286

design. In many applications, such as audio systems, sensor interfaces, and communication devices, the amplifier needs to drive a wide range of load capacitors [2-5]. This requirement poses additional challenges to the design of a stable three-stage amplifier, as the stability can be significantly affected by the value of the load capacitor.

Various solutions have been proposed to increase the bandwidth of three-stage amplifiers stabilized by the Nested Miller Compensation (NMC) method. Most proposed solutions employ two compensation capacitors, but other measures are also applied to improve bandwidth. These measures can be categorized into three main groups:

1. The use of series resistance with the compensation capacitor through active compensation, such as employing a transconductance layer like a common gate in the path of the compensation capacitor.
2. Utilizing feedforward paths to create extra zeros in the transfer function.
3. Employing a negative capacitor to reduce the time constant of intermediate nodes, which can be created by an additional circuit or by utilizing the Miller effect.

Recent advancements have also explored adaptive compensation techniques and hybrid compensation methods that combine both traditional and modern strategies to enhance stability and performance. Techniques such as adaptive biasing and digital-assisted analog compensation are gaining traction, providing more flexibility and robustness against process, voltage, and temperature variations [6-11].

In this paper, I present a novel design for a stable three-stage amplifier that accommodates a wide range of load capacitors. My proposed design addresses these challenges by incorporating innovative techniques to enhance stability and manage various capacitive loads. The effectiveness of my design is validated through rigorous simulations and experimental results.

Numerous articles have been written using these methods, combinations of these methods, or new methods, which can be reviewed in references [6-11]. This paper is organized as follows: Section 2 analyzes the principles of performance enhancement and discusses the main design objectives. Section 3 provides simulation data and circuit layout using 180 nm CMOS technology. Section 4 presents the conclusion.

2. PROPOSED AMPLIFIER

2.1. OTA Schematic

The schematic of the proposed three-stage amplifier is shown in Figure 1. The first stage is a folded-cascode differential amplifier comprising the tail device M_0, input transistors M_{1a}-M_{1b}, current sources M_{2a}-M_{2b}, and cascode devices M_{3a}-M_{3b} and M_{4a}-M_{4b} as the current mirror. The second stage is a noninverting amplifier consisting of M_5-M_7, achieving a positive gain factor and establishing the second-stage transconductance g_{m2} as the product of the transconductance of M_5 and the gain of the current mirror M_{6a}–M_{6b}. The second stage is followed by the common-source amplifier made by M_8 and M_9, providing a rail-to-rail voltage swing at the output. Here, g_{m3} and g_{mf} represent their transconductances, respectively. The feedforward g_{mf} stage through M_9 implements a class-AB output stage with a push-pull strategy, enhancing large-signal and small-signal load driving capabilities [6].

2.2. OTA Block Diagram

Figure 2 displays the small-signal block diagram during normal operation, where the output impedance of various stages is represented by equivalent resistors R_1, R_2, R_3 and capacitors C_1, C_2, C_3. The output terminal drives C_L, which typically has a much higher value than the parasitic C_1, C_2, C_3. The frequency compensation includes the series components R_D and C_D, alongside C_1 and C_2. The Miller capacitor, denoted as C_2, links the source of the common-gate device M3a to the output, adding a g_{mC} stage with input resistance $1/g_{mC}$ to the compensation, preceding v_{O1} in Figure 2.

The proposed compensation strategy additionally includes C_1 to fine-tune the quality factor of non-dominant poles, especially at very small C_L values [8]. Linking the source terminal of M_{3b} to the second stage v_{O2} in Figure 1, these capacitors form additional feedback to sense the gain factor and accordingly adjust the Q–factor, as will be

analyzed later. The local impedance attenuation branch made of R_D and C_D influences the high-frequency impedance at node v_{O1}, providing adaptive control over the location of the non-dominant poles generated [6].

2.3. Transfer Function

The formulas for the transfer function, phase margin, and gain margin, which are similar to those in [8], are as follows:

$$A_v \approx \frac{A_0}{1+\frac{s}{p_{-3dB}}} \cdot \frac{1+\frac{C_{C1}}{g_{mC}}s-\frac{C_{C1}C_{C2}}{g_{mC}g_{m3}}s^2}{1+\left[\frac{1}{g_{mC}}+\frac{1}{g_{m3}}\left(1+\frac{C_L}{C_{C2}}\right)\right]C_{C1}s+\frac{C_{C1}C_L}{g_{mC}g_{m3}}s^2} \approx \frac{A_0\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+\frac{s}{Q\omega}+\frac{s^2}{\omega^2}\right)} \quad (1)$$

Where

$$p_{-3dB} = \frac{1}{R_3C_L+g_{m2}g_{m3}R_1R_2R_3C_{C2}} \quad (2)$$

is the dominant pole. The direct current (DC) gain and gain-bandwidth (GBW) frequency are specified as follows:

$$A_0 = g_{m1}g_{m2}g_{m3}R_1R_2R_3 \quad (3)$$

$$GBW = A_0 \cdot p_{-3dB} = \frac{g_{m1}}{\frac{C_L}{g_{m2}g_{m3}R_1R_2}+C_{C2}} \quad (4)$$

In the context of small to moderate load capacitance (C_L), the gain-bandwidth (GBW) exhibits a gradual alteration. However, a substantial augmentation in load capacitance precipitates a decrease in GBW. This observation suggests that the proposed amplifier, when dealing with hefty capacitive loads, depends on compensation by C_L rather than C_{C2}. The stability of the amplifier is significantly influenced by the first and second non-dominant poles, which are determined by the frequency ω_0 and the quality factor (Q).

$$\omega_0 = \sqrt{\frac{g_{mC}g_{m3}}{C_{C1}C_L}} \quad (5)$$

$$Q = \frac{1}{g_{m3}+g_{mC}\left(1+\frac{C_L}{C_{C2}}\right)}\sqrt{\frac{g_{mC}g_{m3}C_L}{C_{C1}}} \quad (6)$$

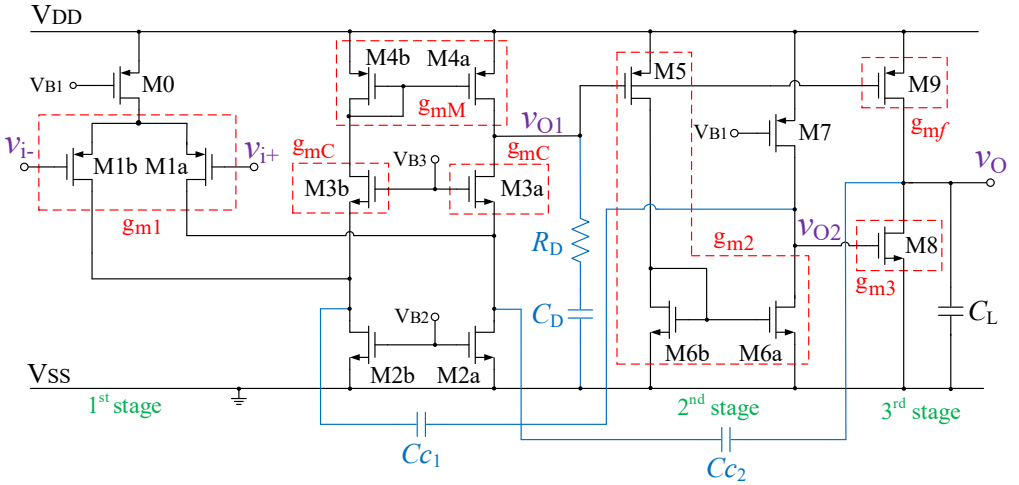

Fig. 1. Schematic of the proposed OTA.

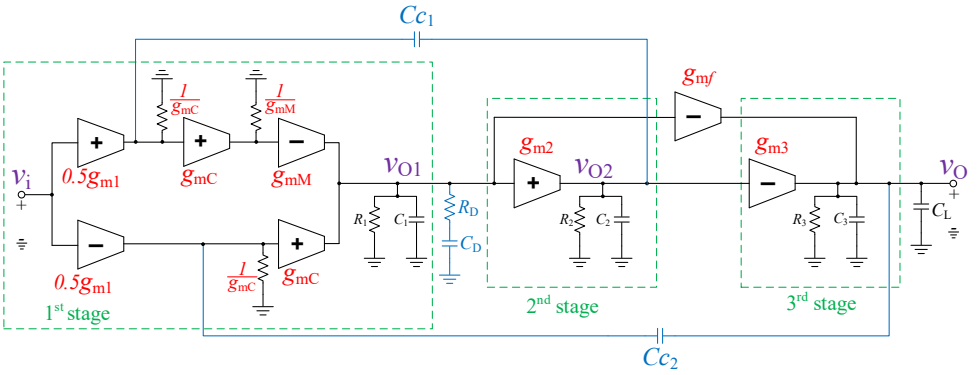

Fig. 2. Small-signal equivalent circuit.

2.4. Analysis of Stability

The gain margin (GM) is a critical parameter in amplifier design, providing a "safety margin" for the gain of the system and ensuring stability under various conditions. A larger gain margin enhances system stability. A positive gain margin indicates a stable system, while a negative gain margin indicates instability. The gain margin equation for this circuit is:

$$GM \approx 20\log\left[\left(\frac{C_{C2}}{C_L}+\frac{1}{g_{m2}g_{m3}R_1R_2}\right).\frac{g_{m3}+g_{mC}\left(1+\frac{C_L}{C_{C2}}\right)}{g_{m1}}\right]-10\log\left[1+4\frac{g_{mC}}{g_{m3}C_{C1}C_L}\left(\frac{C_{C2}}{1+\sqrt{1+4\frac{g_{mC}C_{C2}}{g_{m3}C_{C1}}}}\right)^2\right]$$

$$-10\log\left[1+4\frac{g_{mC}}{g_{m3}C_{C1}C_L}\left(\frac{C_{C2}}{1-\sqrt{1+4\frac{g_{mC}C_{C2}}{g_{m3}C_{C1}}}}\right)^2\right] \quad (7)$$

The frequency of the -3 dB pole is contingent upon the capacitive load (C_L) when C_L is substantial. This implies that the operational transconductance amplifier (OTA) compensation is executed by C_L, rather than C_2, under significant capacitive loads. As inferred from equation (7), the gain margin (GM) is not compromised at large C_L; in fact, GM escalates as C_L increases. For small to moderate capacitive loads, the -3 dB pole frequency is inversely proportional to C_2, resulting in a sufficiently large GM as C_L approaches zero. To increase GM under light loading conditions, it is recommended to augment the ratios of g_{m3}/g_{m1} and C_{C2}/C_{C1}. The gain margin for the amplifier with a large load capacitor, when $C_L >> g_{m2}g_{m3}R_1R_2C_{C2}$, and with a small load capacitor, when $C_L << g_{m2}g_{m3}R_1R_2C_{C2}$, is summarized by the following equations:

$$\lim_{C_L\to\infty} GM \approx 20\log\left(\frac{2g_{mC}C_L}{g_{m1}g_{m2}g_{m3}R_1R_2C_{C2}}\right) \quad (8)$$

$$\lim_{C_L\to 0} GM \approx 20\log\left(\frac{(g_{m3}+2g_{mC})C_{C2}}{g_{m1}C_3}\right)-20\log\left(\frac{\sqrt{1+4\frac{g_{mC}C_{C2}}{g_{m3}C_{C1}}}-1}{\sqrt{1+4\frac{g_{mC}C_{C2}}{g_{m3}C_{C1}}}+1}\right) \quad (9)$$

The phase margin (PM) is a crucial measure of an amplifier's stability, helping to prevent unwanted oscillations and ensuring correct operation under various conditions. The phase margin equation for this circuit is:

$$PM \approx 90^{\circ} - \tan^{-1}\left(\frac{g_{m1}g_{m2}\left[g_{m3}+g_{mC}\left(1+\frac{C_L}{C_{C2}}\right)\right]R_1R_2}{g_{mC}\left[1-g_{m3}C_LC_{C1}\left(\frac{g_{m1}g_{m2}R_1R_2}{g_{m2}g_{m3}R_1R_2C_{C2}+C_L}\right)^2\right]}\cdot\frac{C_{C1}}{g_{m2}g_{m3}R_1R_2C_{C2}+C_L}\right)+\tan^{-1}\left(\frac{2g_{m1}g_{m2}R_1R_2}{\sqrt{1+4\frac{g_{mC}C_{C2}}{g_{m3}C_{C1}}}-1}\cdot\frac{C_{C2}}{g_{m2}g_{m3}R_1R_2C_{C2}+C_L}\right)+\tan^{-1}\left(\frac{2g_{m1}g_{m2}R_1R_2}{\sqrt{1+4\frac{g_{mC}C_{C2}}{g_{m3}C_{C1}}}+1}\cdot\frac{C_{C2}}{g_{m2}g_{m3}R_1R_2C_{C2}+C_L}\right) \quad (10)$$

Unfortunately, it's not feasible to ascertain the minimum phase margin from the given equation. However, when evaluating the phase margin (PM) for both infinite and zero load capacitors, the results are as follows:

$$\lim_{C_L\to\infty} PM \approx 90^{\circ} - \tan^{-1}\left(\frac{g_{m1}g_{m2}+R_1R_2}{C_{C2}}\right) \quad (11)$$

$$\lim_{C_L\to 0} PM \approx 90^{\circ} - \tan^{-1}\left(\frac{g_{m1}(g_{m2}+g_{mC})C_{C1}}{g_{m3}g_{mC}C_{C2}}\right)+\tan^{-1}\left[\frac{2g_{m1}}{g_{m3}\sqrt{4\frac{g_{mC}C_{C2}}{g_{m3}C_{C1}}-1}}\right]+\tan^{-1}\left[\frac{2g_{m1}}{g_{m3}\sqrt{4\frac{g_{mC}C_{C2}}{g_{m3}C_{C1}}+1}}\right] \quad (12)$$

The relevance of the dominant pole to C_L becomes significant as the load approaches infinity, ensuring stability for large capacitive loads, albeit with a trade-off of reduced bandwidth. Referring to equation (11), it is evident that optimizing the parameters g_{m1}, g_{m2}, C_{C1}, and C_{C2} results in a sufficiently elevated phase margin (PM) for heavy capacitive loads. Zeros remain largely unaffected by the load. However, an increase in C_L leads to a decrease in both non-dominant poles and the gain-bandwidth (GBW) product, thereby minimizing stability variations. The poles ultimately transform into a real form, with one pole remaining nearly unchanged and the other declining with the capacitive load at the same GBW rate. This approach can be enhanced by positioning the load-dependent pole of heavy capacitive loads at frequencies beyond the GBW. Favorable stability conditions can be maintained with an enlarged C_{C2}/C_{C1} ratio. When utilizing a precisely tailored compensation network, the minimum value of C_L will not be constrained by the PM. The dominant pole is solely influenced by C_{C2} when the condition $C_L << g_{m2}g_{m3}R_1R_2C_{C2}$ is met. Reducing C_L results in an increase in ω_0, as evident from equation (5). This leads to a larger phase margin if its contribution surpasses the GBW increase in equation (4). In practice, stability conditions are predominantly governed by the GM rather than PM for lower capacitive loads.

3. POST-LAYOUT SIMULATION RESULT

The proposed three-stage amplifier, as illustrated in Figure 1, is simulated using standard 180 nm CMOS technology, with the circuit biased at a nominal voltage of 1.8 V. Figure 3 depicts the meticulously designed amplifier layout, optimized to minimize dead space. Typically, the layout design is rectangular or square. PMOS and NMOS transistors, each with different body voltages, are placed within a guard ring to prevent cross-talk interference and reduce noise in the body.

In CMOS technology, NMOS transistors are constructed on a p-type substrate, while PMOS transistors require the creation of an N-Well, a relatively deep n-type region that serves as their body. The substrate is connected to the lowest circuit voltage, and the N-Well is connected to the transistor's source, ensuring that both the substrate and N-Well are reverse biased relative to each other. This configuration ensures that all sources and drains of the transistors are in a reverse bias state with respect to their body, preventing any current from passing through their P-N junction.

The capacitors and resistors used in the design are Metal-Insulator-Metal (MIM) capacitors and rnhpoly (N+ poly resistor without silicide) resistors, respectively. The proposed three-stage amplifier, shown in Figs. 1 and 3, was designed using Cadence Virtuoso software. This design employs a 0.18 μm Mixed-Signal SALICIDE process (1P6M+, 1.8V/3.3V) and utilizes the BSIM3 model (V3.24). Additionally, Spectre version 6.0.2.247 was used for the simulations.

The layout of this amplifier occupies 0.0026 mm², and its current consumption is 23.38 μA. Table 1 presents the dimensions of the transistors and the values of the capacitors and the compensation resistor. The total capacitance of the compensation capacitors is 0.87 pF, and the resistance value is 27 kΩ. The dimensions of the transistors are

small, and no multipliers are used for the transistors, resulting in a compact layout design. The supply voltage is 1.8 V, with bias voltages set to 1.15 V, 0.5 V, and 0.75 V for Bias Voltage V_{B1}, V_{B2}, and V_{B3}, respectively. The DC voltage for frequency response analysis is set to 0.45 V.

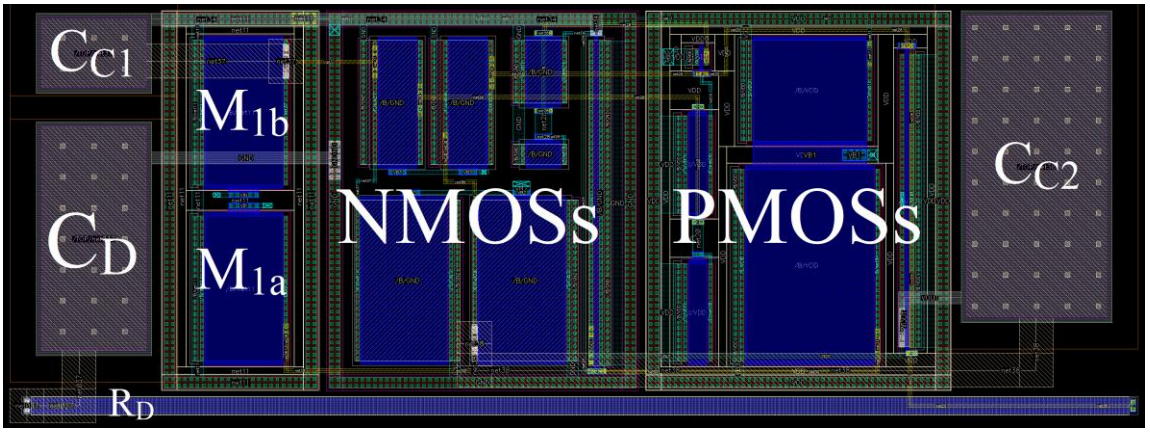

Fig. 3. The designed layout of the proposed three-stage amplifier.

Table 1. Transistor dimension and Small-Signal Parameters of the OTA and Compensation Network

Stage #	Transistor	W/L	Parameter	Value
First	M_0	7.7 µ/8.6 µ	g_{m1} g_{mC}	20 µA/V 43 µA/V
	M_{1a}-M_{1b}	11.1 µ/5.9 µ		
	M_{2a}-M_{2b}	12.3 µ/6.6 µ		
	M_{3a}-M_{3b}	9.5 µ/2.9 µ		
	M_{4a}-M_{4b}	7.5 µ/1.4 µ		
Second	M_5	1.3 µ/0.2 µ	g_{m2}	65 µA/V
	M_{6a}	1.6 µ/2.6 µ		
	M_{6b}	4.8 µ/2.6 µ		
	M_7	14.7 µ/9.8 µ		
Third	M_8	24.8 µ/0.2 µ	g_{m3}	322 µA/V
	M_9	22.4 µ/0.2 µ	g_{mf}	276 µA/V
Compensation Element		R_D		27 kΩ
		C_D		280 fF
		C_{C1}		90 fF
		C_{C2}		500 fF

Figure 4 illustrates the frequency response of the open-loop simulation across various load capacitances (C_L), ranging from 0 to 100 nF. The amplifier demonstrates a DC gain exceeding 100 dB, with the simulation yielding a peak value of 119.3 dB. The average unit gain frequencies are measured as 4.872 MHz for no-load, 2.4 MHz for 0.1 nF, and 90.11 kHz for 100 nF loads. This data shows that the gain-bandwidth product (GBW) inversely correlates with the load capacitance, indicating that as C_L increases, the GBW decreases, consistent with the amplifier's expected behavior.

Figure 5 depicts the frequency response for a load capacitance of 500 pF across various process corners, accounting for temperature variations. The corner analysis ensures that the MOSFETs in the amplifier will perform reliably under different manufacturing and environmental conditions. The simulation results in Figure 5 confirm the robustness and reliability of the proposed amplifier across all expected operating conditions.

Figure 6 shows the measured output settling behavior for external load capacitances ranging from 0 to 100 nF. The settling time represents the duration required for the amplifier to stabilize after a change in the input signal. For

this measurement, the amplifier was configured as a buffer with an input step voltage of 0.4 V. The amplifier remains stable across all tested load capacitances. The 1% settling times were recorded as 0.48 µs for a 100 pF load and 17.53 µs for a 50 nF load, demonstrating effective stability and performance of the amplifier with varying capacitive loads.

Table 2 summarizes the performance criteria of the proposed three-stage amplifier and compares it with recent works. The average 1% settling time for the proposed amplifier was measured at 0.29 µs, 1.37 µs, and 19.92 µs for load capacitors of 0 pF, 500 pF, and 100 nF, respectively. Among the compared works, only [7] demonstrates a shorter settling time for a 100 nF load capacitor. The Figure of Merit (FOM) criteria, as defined in Table 2, assess both large and small signal performance based on factors such as area, quiescent current (IDD), slew rate (SR), bandwidth, and the ratio of maximum to minimum load capacitance (CL,max/CL,min).

In terms of gain and area, the proposed design outperforms all cited studies and maintains acceptable current consumption. Specifically, the proposed amplifier demonstrates a significantly higher DC gain (119.3 dB) compared to others, while having a compact area (0.0026 mm²). The design achieves a high Figure of Merit in both IFOMS and IFOML metrics, indicating superior performance in terms of bandwidth and slew rate relative to current consumption.

For different configurations, the FOMs are evaluated under external loadings of 0 pF, 500 pF, and 100 nF. The proposed amplifier exhibits superior performance by producing infinite values for LR-IFOMLA and LR-IFOMSA, indicating an unlimited CL,max/CL,min ratio. In other FOM metrics such as IFOMS, IFOML, IFOMSA, and IFOMLA, the proposed amplifier also outperforms competing designs, reflecting a higher merit ratio compared to the referenced works. Notably, the high values of FOMSA and FOMLA suggest that the amplifier excels in balancing gain, bandwidth, and area efficiency.

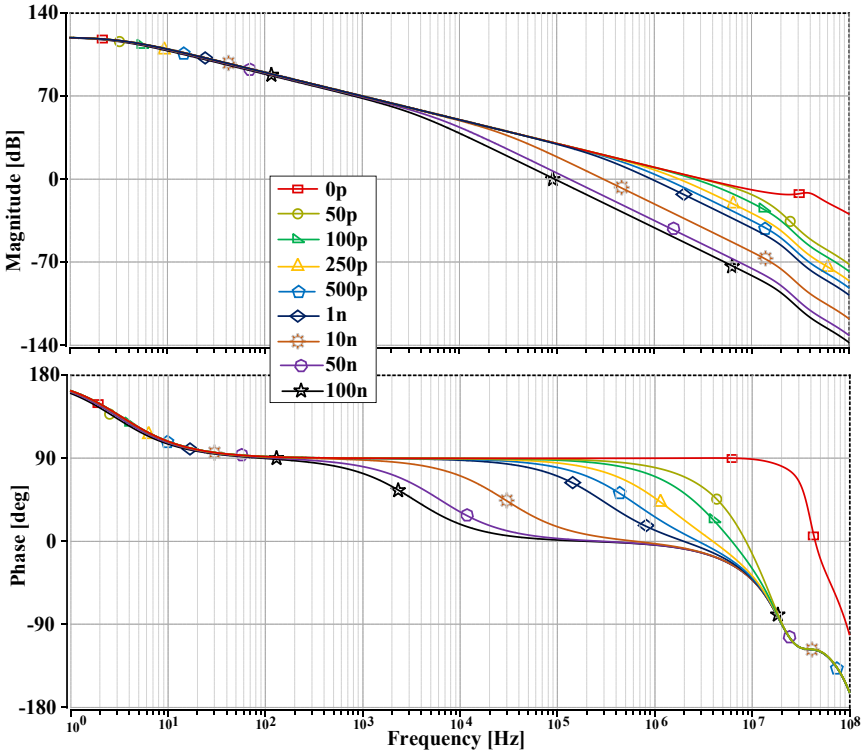

Fig. 4. Simulated frequency response of various load capacitors (C_L).

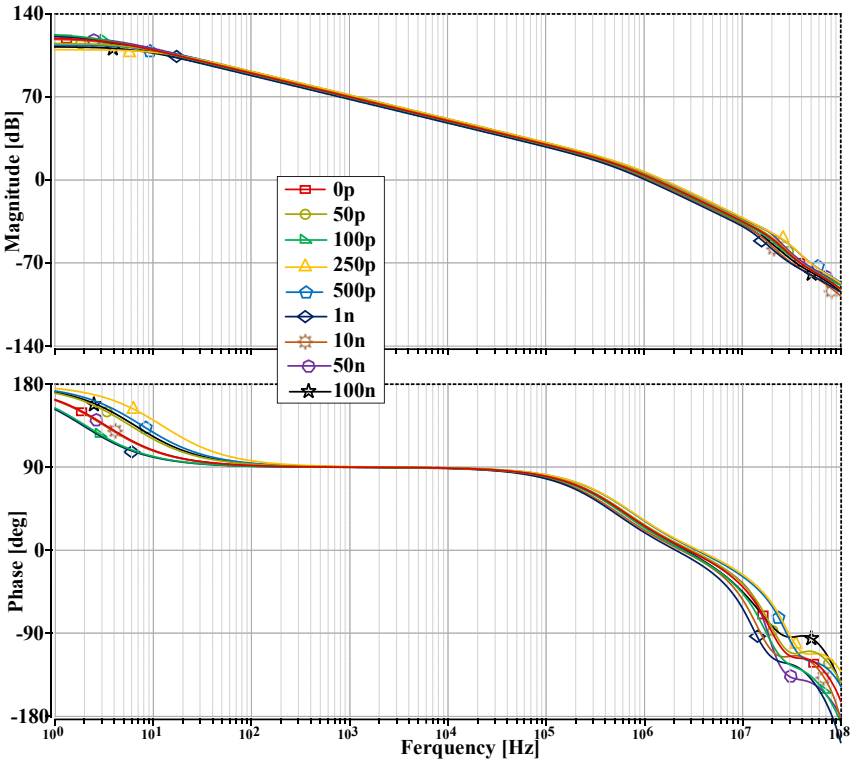

Fig. 5. Simulated frequency response for a load capacitance (CL) of 500 pF at different process corners.

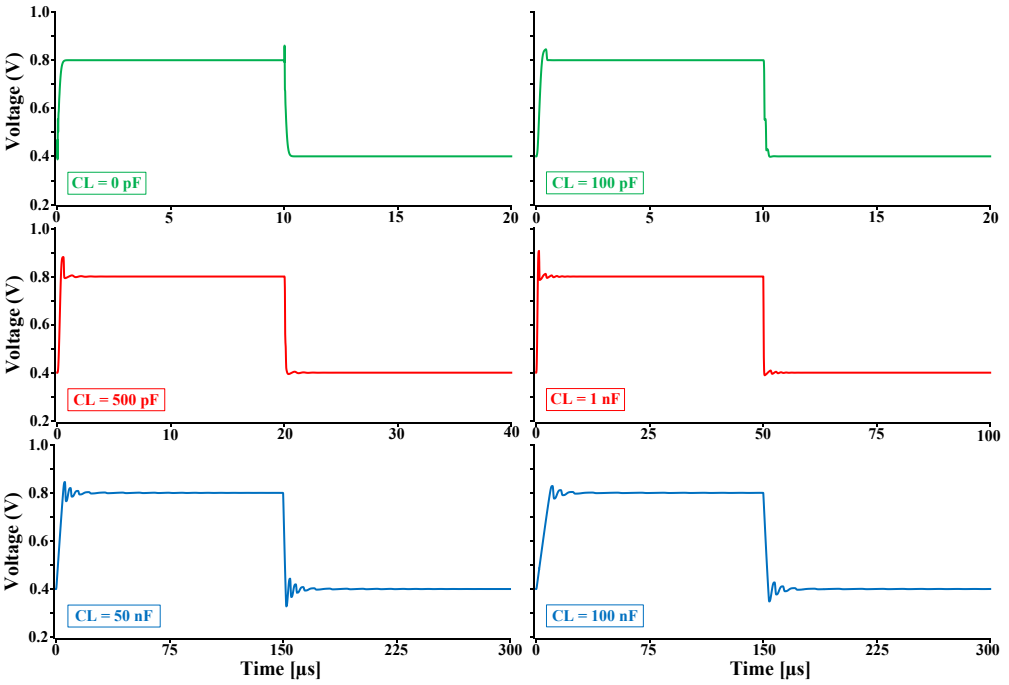

Fig. 6. Measured large-signal settling response from 0 to 100-nF load capacitor.

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Table 2. Performance Parameters and Comparison of This Work to Recent Three-Stage Amplifiers

	2020 [9]	**2020 [6]**		**2022 [7]**			**2024 [8]**			**This work**		
Process [nm]	130	180		65			180			180		
Area [mm^2]	0.006	0.0053		0.0028			0.0055			0.0026		
I_{DD} [µA]	185	10.97		13.1			25			23.4		
A_0 [dB]	72	100.4		100			115			119.3		
Total C_C [pF]	0	1.4		1			1			0.87		
C_L [nF]	4.45-50	0.01	100	0.0	0.5	100	0.0	0.47	100	0.0	0.5	100
$C_{L,max}/C_{L,min}$	11.3	10000		∞			∞			∞		
1% ts [µs]	0.28-4.62	0.83	38	0.62	6.3	16.8	1.8	1.7	19	0.29	1.37	19.9
GBW [MHz]	5.41-0.46	1.22	0.16	18.69	0.705	0.022	4.40	1.12	0.079	2.87	1.24	0.09
SR [V/µs]	0.49-0.04	0.699	0.014	3.52	0.6	0.0044	1.60	1.60	0.021	2.03	1.68	0.045
$IFOM_S$	124.3	1.112	145.9	0	29.97	168	0	21.06	316	0	26.5	384.6
$IFOM_L$	10.81	0.637	127.62	0	22.95	33.66	0	30.08	84	0	35.9	192.3
$IFOM_{SA}$	20721	209.9	275193	0	9632	60104	0	3828	57455	0	10191	147929
$IFOM_{LA}$	1801	120.2	24079	0	8196	12021	0	5469	15273	0	13806	73964
LR-$IFOM_{SA}$	232904	209835	27519	∞			∞			∞		
LR-$IFOM_{LA}$	20243	120225	2408	∞			∞			∞		

$$IFOM_S = \frac{GBW \cdot C_{L,max}}{I_{DD}}\left[\frac{MHz \cdot pF}{\mu A}\right] \qquad IFOM_L = \frac{SR \cdot C_{L,max}}{I_{DD}}\left[\frac{V/\mu s \cdot pF}{\mu A}\right] \qquad IFOM_{SA} = \frac{GBW \cdot C_{L,max}}{I_{DD} \cdot Area}\left[\frac{MHz \cdot pF}{\mu A \cdot mm^2}\right]$$

$$IFOM_{LA} = \frac{SR \cdot C_{L,max}}{I_{DD} \cdot Area}\left[\frac{V/\mu s \cdot pF}{\mu A \cdot mm^2}\right] \qquad LR - IFOM_{SA} = \frac{GBW}{I_{DD} \cdot Area} \cdot \frac{C_{L,max}}{C_{L,min}}\left[\frac{MHz}{\mu A \cdot mm^2}\right] \qquad LR - IFOM_{LA} = \frac{SR}{I_{DD} \cdot Area} \cdot \frac{C_{L,max}}{C_{L,min}}\left[\frac{V/\mu s}{\mu A \cdot mm^2}\right]$$

4. CONCLUSIONS

Multistage amplifiers face significant stability challenges due to the variable positions of poles and zeros, which are influenced by capacitive loads (C_L). To tackle these challenges, we have introduced a novel frequency compensation scheme designed to stabilize a three-stage amplifier without imposing a limit on C_L. This approach leverages Miller capacitors in series with integrated current buffers and incorporates a feedback network from the second stage to the first. This feedback mechanism effectively adjusts the Q-factor of non-dominant poles, thereby enhancing stability across a broad range of capacitive loads. The amplifier, implemented using standard 180 nm CMOS technology, was thoroughly validated through rigorous simulations. The results highlight substantial improvements in both small-signal and large-signal figures of merit, demonstrating excellent performance across various capacitive loads. Notably, the amplifier's ability to handle a virtually unlimited range of capacitive loads marks a significant advancement in multistage amplifier design. In summary, our innovative frequency compensation approach not only addresses critical stability issues but also provides the capability for limitless capacitive load drivability. This advancement has the potential to revolutionize the design and application of multistage amplifiers in a wide array of electronic devices.

Declaration

We acknowledge that we used ChatGPT to enhance the academic writing of our manuscript while ensuring the originality and integrity of our work.

Transparency Statement

The data supporting this study are available upon reasonable request to the corresponding author, subject to ethical and confidentiality considerations.

Acknowledgments

We would like to express our gratitude to all individuals who contributed to this project.

Declaration of Interest

The authors declare that they have no competing interests.

Funding

This research received no specific grant from any funding agency, commercial, or not-for-profit sectors.

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