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A Low-Power and Low-Noise Fully Integrated Amplifier for Neurodegenerative Disease Detection

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ABSTRACT

Today, medical equipment provides a suitable and innovative solution for physicians and specialists in diagnosing various neurodegenerative diseases, such as Parkinson's, Alzheimer's, and epilepsy. The accurate recording and analysis of neural signals are critical for understanding the functioning of the brain and nervous system. Designing a block of a neural signal recording system with medical and localized applications to amplify vital and neural signals of the body, including brain and heart signals, significantly aids in the accurate diagnosis of disease types and improves treatment planning. This paper presents the design of a low-power, low-noise preamplifier circuit specifically intended for recording delicate neural signals, which are often affected by interference and signal distortion. By selecting an amplifier with an RFC (Resistive Feedback Capacitor) structure and similar power consumption characteristics, the proposed design achieves high gain performance while reducing overall noise levels. Careful selection of the circuit structure not only suppresses ripple effects present in neural signals but also optimizes power consumption, lowers the noise floor, and minimizes silicon area, making the circuit suitable for integration in portable or implantable medical devices. The proposed circuit has been designed using 180 nm CMOS technology provided by TSMC under the BSIM library and has been fully simulated using HSPICE 2008 software to validate its performance and effectiveness.

1. INTRODUCTION

Neurological and brain disorders can often be far more peculiar, rare, and distressing than common and familiar ailments in the realm of neuroscience. According to statistics, approximately fifty million people worldwide suffer from neurological injuries and strokes [1-5]. These injuries, resulting from disease, accidents, or infections affecting the brain, spinal cord, or nerves, are collectively known as neurological impairments. Such impairments can significantly impact all-natural bodily functions, from eating and breathing to speech and movement. Consequently,

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researchers strive to design and implement diagnostic kits and systems capable of automatically recording and analyzing neural and brain signals [6].

Received brain signals manifest as one-dimensional, time-varying oscillations that reflect the dynamic electrical activity of neural tissue. In a resting state, without the execution of specific tasks, these brain signals typically appear continuous and relatively uniform. The oscillation frequency of these signals correlates with the individual's level of alertness, concentration, mental state, and emotional condition. Such signals can be recorded using Intracranial Electroencephalography (iEEG) methods, which provide essential information for predicting the onset timing of seizures and for diagnosing other neurological conditions. The signal energy is primarily concentrated within the frequency range of 200 to 600 hertz, with amplitudes varying from approximately 30 microvolts (μV) to 1.5 millivolts (mV), depending on the size and placement of the electrodes employed in the iEEG recording process [7].

Given the unpredictable and often sudden nature of neurological disorders, amplifiers used in these systems must maintain continuous capability to record and amplify neural signals over prolonged periods, all while minimizing power consumption to extend device longevity. Furthermore, due to the inherently low amplitude of neural and brain signals, minimizing noise is a critical design parameter. Therefore, the input-referred noise must be kept as low as possible to prevent interference and ensure accurate signal analysis. The following section provides a detailed overview of the design and specifications of the proposed preamplifier block.

2. GENERAL STRUCTURE OF THE PREAMPLIFIER

According to the structure depicted in Figure 1, the preamplifier designed for neural signal recording consists of an amplification circuit to enhance the amplitude of recorded weak signals. It prepares these signals for processing and specifically targets a particular frequency range where the signal energy, FR, is embedded [6, 7].

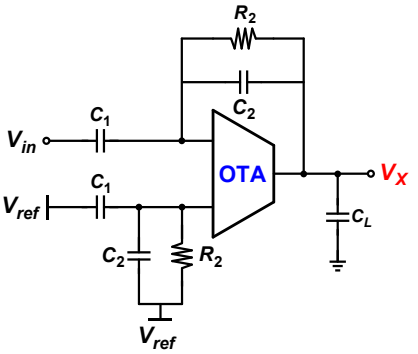

Fig. 1. Block diagram of the neural signal pre-amplifier circuit

The desired pre-amplifier stage is based on an OTA (Operational Transconductance Amplifier) and has a capacitive feedback structure as shown in Figure 1. This pre-amplifier is designed based on the OTA and produces an output current proportional to the difference between the input voltages, where Gm is the constant of this proportionality. The midband gain (Am) of the amplifier is determined by the ratio C_1/C_2, and its bandwidth is approximately Gm/(AmCL) when $C_1 \cdot C_L \gg C_2$

The recorded signal is capacitively coupled to the circuit through capacitor C1, which eliminates the DC offset generated at the electrode-tissue interface and allows only the AC component of the recorded signal to pass through. This prevents the amplifier from saturation due to the high gain required to amplify the weak recorded signals [8-9].

The resistor R2 in the feedback loop determines the lower cutoff frequency of the amplifier. These resistors are implemented on-chip as pseudo-resistors using PMOS and NMOS transistors [10].

The transfer function from the input to the output of the pre-amplifier stage is derived as follows:

$$\frac{V_X}{V_{in}} = \frac{C_1}{C_2} \cdot \frac{\frac{1-sC_2}{G_m}}{\left(\frac{1}{sR_2C_2}+1\right)\left(s\frac{C_LC_1}{G_mC_2}+1\right)} = A_M \frac{1-s/(2\pi f_Z)}{\left(1+\frac{2\pi f_L}{s}\right)\left(1+\frac{s}{2\pi f_H}\right)} \quad (1)$$

According to equation (1), the midband gain Am is determined by the expression C^1/C_2, and the gain between the lower and upper cutoff frequencies is flat. The lower cutoff frequency is set by the resistance R_2 and capacitor C_2. Additionally, the upper cutoff frequency of the circuit is determined by the load capacitance C_L, the transconductance of the OTA, and the midband gain of the amplifier. Moreover, the presence of capacitive feedback introduces a positive zero at frequency f_z, which can be shifted to very high frequencies by choosing $C_2 \ll \sqrt{(C_1\ CL)}$. Figure 2 illustrates the frequency response of the gain of the preamplifier circuit [11].

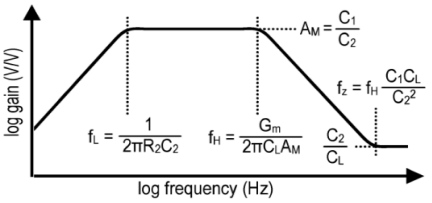

Fig. 2. The frequency response of the gain of the pre-amplifier circuit.

Figure 3 illustrates the placement of the noise sources present in the preamplifier circuit. Figure 4 depicts the various components of the overall output noise of the amplifier in the case where both noise sources V_{nia} and V_{nR} are white noise. The OTA noise is primarily situated within the frequency range between the lower and upper cutoff frequencies. The noise from V_{nR} also dominates for frequencies lower than the corner frequency f_{corner}.

If the resistance R_2 is implemented using a real resistor, the noise power spectral density is given by:

$$v_{nR}^2(f) = 4kTR_2 \tag{2}$$

If C1 ≫ C2, Cin, the corner frequency is approximately:

$$f_{corner} \approx \sqrt{\frac{3C_L}{2C_1} f_L f_H} \tag{3}$$

To mitigate the noise from R_2, the corner frequency must be significantly lower than the upper cutoff frequency of the entire circuit. To this end, the amplifier should be designed such that the following condition is met:

$$\frac{C_L}{C_1} \ll \frac{2f_H}{3f_L} \tag{4}$$

If the noise from the R_2 resistance is negligible, i.e., $f_{corner} \ll f_H$ *and* $C_1 \gg C_2$, C_{in}, then the rms output noise voltage of the amplifier in Figure 4 is limited by the noise from the OTA.

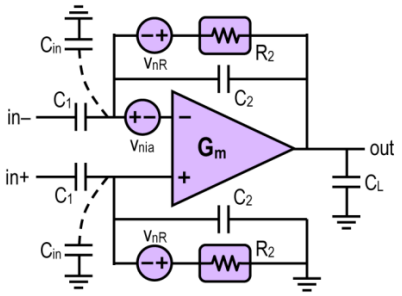

Fig. 3. Noise source modeling for the preamplifier circuit

The input-referred thermal noise power spectral density of the OTA is given by:

$$v_{nia}^2(f) = \frac{16kT}{3g_{m1}}\left(1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right) \tag{5}$$

where gm1 is the transconductance of transistors M1,2, gm3 is the transconductance of transistors M(3-6), and gm7 is the transconductance related to transistors M7,8.

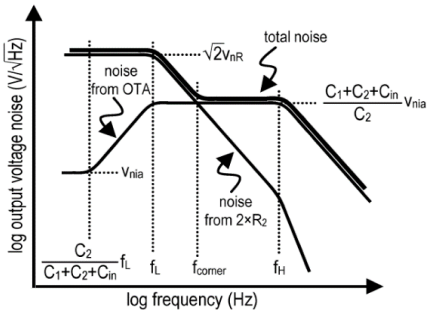

Fig. 4. Output noise of the preamplifier circuit as a function of frequency

2.1. Selecting the structure for the OTA

The folded-cascode (FC) amplifier has become one of the most widely used structures, both as a single-stage and as the first stage in multi-stage CMOS low-voltage designs, due to its high voltage gain and large signal swing. Furthermore, the FC with PMOS input has much wider application than the FC with NMOS input, owing to its higher nondominant poles, lower flicker noise, and better common-mode input range. In switched-capacitor circuits, the input switching operation can be performed using a single NMOS transistor.

The conventional FC amplifier is shown in Figure 5. Note that transistors M3 and M4 carry the largest currents and, in many designs, have the highest transconductance. However, their role is to provide a folding node for the small signal currents generated by the input drivers (M1 and M2). Therefore, the modified folded-cascode structure shown in Figure 6 is designed. In this structure, M3 and M4 are used as the driver transistors. The input drivers (M1 and M2) in Figure 5 are transformed into M1a, M1b, M2a, and M2b in Figure 6. These transistors carry equal and fixed currents (Ib/2). The transistors M3 and M4 in Figure 5 are also transformed into M3a, M3b, M4a, and M4b in Figure 6 to form two current mirrors with a K:1 ratio. The cross-coupling of these two current sources ensures that the small signal currents added at the sources of M5 and M6 are in-phase. Finally, the transistors M11 and M12 are sized similarly to M5 and M6, and their use ensures that the drain potentials of M3a, M3b, M4a, and M4b are equal, resulting in better matching [11-15].

2.2. Recycled Folded Cascode (RFC)

In order to qualitatively demonstrate the improved aspects in the RFC structure, it is assumed that all transistors operate in the saturation region.

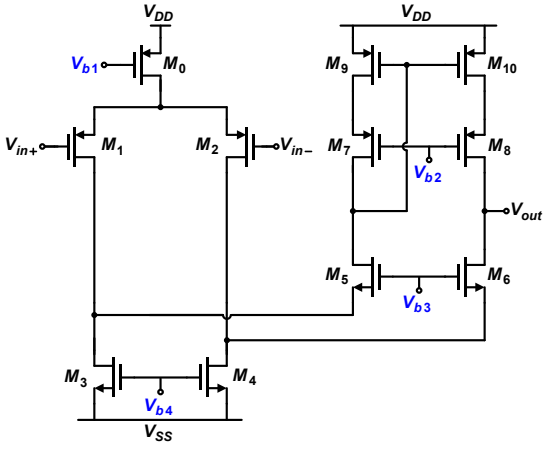

Fig. 5. Conventional cascode amplifier

Furthermore, the current gain K is chosen to be 3. This ensures that the power consumption is identical for both the FC and RFC structures. It should also be noted that the current flowing through transistors M5 to M10 is a function of K. For K≠3, the transistors M5 to M10 must be rescaled to achieve the same power consumption and area as the FC circuit when K=3.

The analyses presented hereafter are valid for both the single-ended and differential amplifier configurations. However, the focus is primarily on the fully differential structure.

2.3. Small-signal transconductance

The transconductance of the amplifier, Gm, can be obtained by using the short-circuit output current with respect to the input. The desired results for the RFC and FC structures are shown in Equations (6) and (7), respectively:

$$G_{m.RFC} = g_{m1a}(1 + K) \quad (6)$$

$$G_{m.FC} = g_{m1} \quad (7)$$

Considering that the size of M1 is twice the size of M1a and draws twice the current (gm1=2gm1a), and substituting the value of K, it can be concluded that the RFC transconductance is twice that of the FC, for the same power consumption. In other words, for the same power consumption, the gain-bandwidth product (GBW) of the RFC is approximately twice that of the FC structure, and consequently, it has twice the speed [13-14].

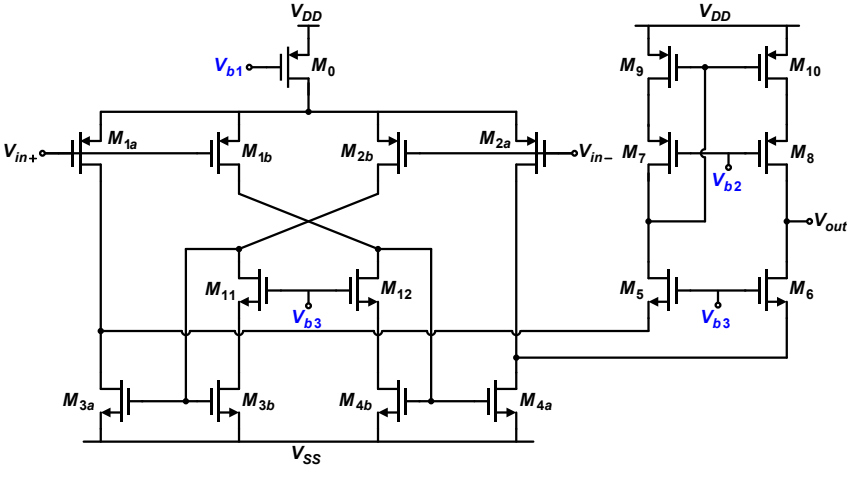

Fig. 6. Recycled Folded Cascode (RFC)

2.4. Low Frequency Gain

The low frequency gain of OTAs is typically expressed as the product of the small-signal transconductance, Gm, and the low-frequency output impedance, Ro. It has been shown that $G_{m.RFC} = 2G_{m.FC}$ which leads to an improvement in gain by approximately 6 dB for the same output impedance. However, the output impedance of the RFC has been significantly improved compared to the FC, as observed in the following relationships:

$$Ro_{FC} \cong g_{m6}r_{ds6}(r_{ds2} \| r_{ds4}) \| g_{m8}r_{ds8}r_{ds10} \quad (8)$$

$$Ro_{RFC} \cong g_{m6}r_{ds6}(r_{ds2a} \| r_{ds4a}) \| g_{m8}r_{ds8}r_{ds10} \quad (9)$$

The increase in gain due to the higher output impedance of the RFC structure is attributed to the increased rds of transistors M2a and M4a, meaning that these transistors draw less current compared to their counterparts (M2 and M4) in the FC structure. Consequently, the overall low-frequency gain exhibits an improvement of 8-10 dB compared to the FC structure.

This additional gain offers two significant advantages. Firstly, it reduces the impact of static offset errors due to the increased gain. Secondly, it improves the PSRR (Power Supply Rejection Ratio) of the RFC compared to the FC structure. The PSRR is defined as the ratio of the gain of the noise injected from the power supply to the gain of the input signal. Both the RFC and FC structures have the same power supply noise gain, but the loop gain of the RFC is higher, leading to an enhanced PSRR performance. Furthermore, the increased GBW (Gain-Bandwidth) of the RFC structure further improves the PSRR at higher frequencies compared to the FC structure [12-15].

2.5. Slew Rate

The slew rate is derived from the maximum output current that charges the load capacitor. It is obtained such that when a large voltage is applied to the V(in+) input, Mb1 and Ma1 are turned off, followed by the turn-off of Ma4 and Mb4, resulting in a high drain voltage for these transistors. This, in turn, causes M6 to turn off and Ma2 to enter the deep triode region. Consequently, the current of Mb2 is transferred to the output through the gains of K and K-1, and the slew rates for the RFC and FC amplifiers are defined in Equations 10 and 11, respectively [14-18].

$$S.R_{RFC} = \frac{2KI}{C_L} \tag{10}$$

$$SR_{FC} = \frac{2I}{C_L} \tag{11}$$

2.6. Phase Margin

To achieve an appropriate phase margin, attention must be paid to the location of the zeros and poles of the RFC amplifier. The first pole is related to the output impedance and capacitance, the second pole is related to the source MOSFETS M5 and M6, and the third pole is related to the current mirror transistors. Opposing this third pole, there is also a mirror zero with a value of K+1 times the mirror pole. To maintain a suitable phase margin for this amplifier, the third pole should be sufficiently far from the unity-gain frequency, ωGBW, such that:

$$|\omega_{P3}| \geq |3\omega_{GBW}| \rightarrow K \leq \sqrt{\frac{C_L g_{mb3}}{3 g_{ma1} C_{gsb3}}} - 1 \tag{12}$$

where ωP3 is the third pole and ωGBW is the unity-gain frequency of the amplifier. Additionally, gmb3 and Cgsb3 are the transconductance and gate-source capacitance of MOSFET Mb3, respectively.

2.7. Noise

In many applications, such as audio amplifiers, continuous-time filters, and data converters, noise can act as a limiting factor in the design. The maximum rms noise current observed at the output of a MOSFET is given by:

$$\overline{i_o^2} = \left[4k_B T\gamma gm + \frac{K_F I_D}{C_{ox} L^2 f}\right].\Delta f \tag{13}$$

The first and second terms represent the thermal noise and flicker noise, respectively. For comparison, the thermal and flicker noise components are examined separately. The referred-to-input thermal noise for the FC and RFC amplifiers is, respectively:

$$\overline{v_{iT.FC}^2} = \frac{8k_B T\gamma}{gm_1}\left[1 + \frac{gm_3}{gm_1} + \frac{gm_9}{gm_1}\right].\Delta f \tag{14}$$

$$\overline{v_{iT.RFC}^2} = \frac{8k_B T\gamma}{gm_{1a}}\left[\frac{(1+K^2)}{(1+K)} + \frac{gm_{3a}}{gm_{1a}} + \frac{1}{(1+K)}\frac{gm_9}{gm_{1a}}\right].\Delta f \tag{15}$$

By substituting gm1a with gm1 and gm3a with gm3, and the value of K, equation (16) becomes:

$$\overline{v_{iT.RFC}^2} = \frac{8k_B T\gamma}{gm_1}\left[\frac{5}{4} + \frac{3gm_3}{4gm_1} + \frac{1}{4}\frac{gm_9}{gm_1}\right].\Delta f \tag{16}$$

The flicker noise expressions for the FC and RFC structures are, respectively, given by the following equations:

$$\overline{v_{if.FC}^2} = \frac{K_{FP}}{\mu_p C_{ox}^2 W_1 L_1 f}\left[1 + 2\frac{K_{FN}}{K_{FP}} + \left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_9}\right)^2\right].\Delta f \quad (17)$$

$$\overline{v_{if.RFC}^2} = \frac{K_{FP}}{\mu_p C_{ox}^2 W_{1a} L_{1a}(1+K) f}\left[\frac{(1+K^2)}{(1+K)} + K\frac{K_{FN}}{K_{FP}} + \left(\frac{L_{1a}}{L_{3a}}\right)^2 + \frac{(K-1)}{(1+K)}\left(\frac{L_{1a}}{L_9}\right)^2\right] \quad (18)$$

The modifications made to the structure of the FC to obtain the RFC structure were limited to the width of the transistors, and no changes were made to the length of the transistors. Therefore, by substituting expressions of W1 for W1a and replacing the value of K, the following equation is obtained for the average squared noise voltage $\overline{v_{if.RFC}^2}$.

$$\overline{v_{if.RFC}^2} = \frac{K_{FP}}{\mu_p C_{ox}^2 W_1 L_1 f}\left[\frac{5}{4} + 1.5\frac{K_{FN}}{K_{FP}} + \left(\frac{L_1}{L_3}\right)^2 + \frac{1}{4}\left(\frac{L_1}{L_9}\right)^2\right].\Delta f \quad (19)$$

Given the above equations, since the two terms present in $\overline{v_{if.RFC}^2}$ and $\overline{v_{iT.RFC}^2}$ are smaller than their counterparts in $\overline{v_{if.FC}^2}$ and $\overline{v_{iT.FC}^2}$, it can be concluded that the RFC structure exhibits lower noise compared to the FC structure.

3. PREAMPLIFIER CAPACITOR AND RESISTOR CALCULATION

After designing the required OTA used in the preamplifier structure, the next step is to design the entire section and determine the values of the capacitor and resistor used to achieve the desired specifications listed in Table 1.

Table 1. Preamplifier Specifications

Parameter	Value
Gain	$\geq$ **40 dB**
Bandwidth	**200 Hz − 600 Hz**
C_L	**1 pF**

To achieve the specified lower cutoff frequency, the values of the resistor R2 and capacitor C2 need to be calculated according to the following equation:

$$F_L = \frac{1}{2\pi R_2 C_2} \xrightarrow{(f_L = 200\ Hz)} 200 = \frac{1}{2\pi R_2 C_2} \xrightarrow{C_2 = 0.1\ pF} R_2 = \frac{1}{2\pi \times 200 \times 0.1\ pF} = 7.95\ G\Omega \quad (20)$$

As can be observed, the value of the resistor R2 is extremely high and must be implemented within the integrated circuit. The dimensions of the transistors forming the pseudo-resistor R2 to achieve a resistance of 7.95 GΩ are provided in Table 3.

In the preamplifier circuit, considering the relationship in equation (1) to achieve a gain greater than 40 dB and the potential attenuation in the overall gain by the bandpass filter, the value of the capacitor C1 must be designed according to equation (21) to meet the above requirements.

$$A_M = \frac{C_1}{C_2} \xrightarrow{(A_M \geq 40\ dB)} 10^{\frac{60}{20}} = \frac{C_1}{0.1\ pF} \xrightarrow{C_2 = 0.1\ pF} 10^3 = \frac{C_1}{0.1\ pF} = 100\ pF \quad (21)$$

Additionally, the upper cutoff frequency of the preamplifier circuit can be obtained from equation (22). As can be seen, this frequency depends on the load capacitance CL, the transconductance of the amplifier Gm, and the midband gain Am [11-13].

$$f_H = \frac{G_m}{2\pi C_L A_M} \quad (22)$$

4. SIMULATION RESULTS

This amplifier was designed with a gain of 27.72 dB in the 180 nm TSMC manufacturing technology. The frequency response of the input-to-output gain of the designed recycling feedback amplifier can be observed in Figure 7. Additionally, the dimensions of the amplifier circuit transistors and the designed bias are provided in Table 2. For the amplifier, the phase margin is 80.75 degrees, the slew rate at the rising edge is 100 V/ns, and the slew rate at the falling edge is 26 V/ns, which can be observed in Figure 8. Figure 9 shows the value of the input-referred noise spectrum, and the total input-referred noise value is 260 $\frac{V^2}{Hz}$ Hz.

Table 2. Dimensions of the Amplifier Circuit Transistors and Bias

Main OTA											
M	W (µm) /L (µm)	Tr.	M	W (µm) /L (µm)	Tr.	M	W (µm) /L (µm)	Tr.	M	W (µm) /L (µm)	**Tr.**
1	0.3/3	$M_{3b.4b}$	4	0.46/0.36	$M_{11.12}$	2	0.66/0.36	$M_{1a.2a}$	4	1.25/0.36	$\mathbf{M_0}$
8	0.46/0.36	$M_{5.6}$	16	0.36/0.36	$M_{7.8}$	1	0.3/0.9	$M_{3a.4a}$	2	0.72/0.36	$\mathbf{M_{1b.2b}}$
									8	0.34/0.36	$\mathbf{M_{9.10}}$

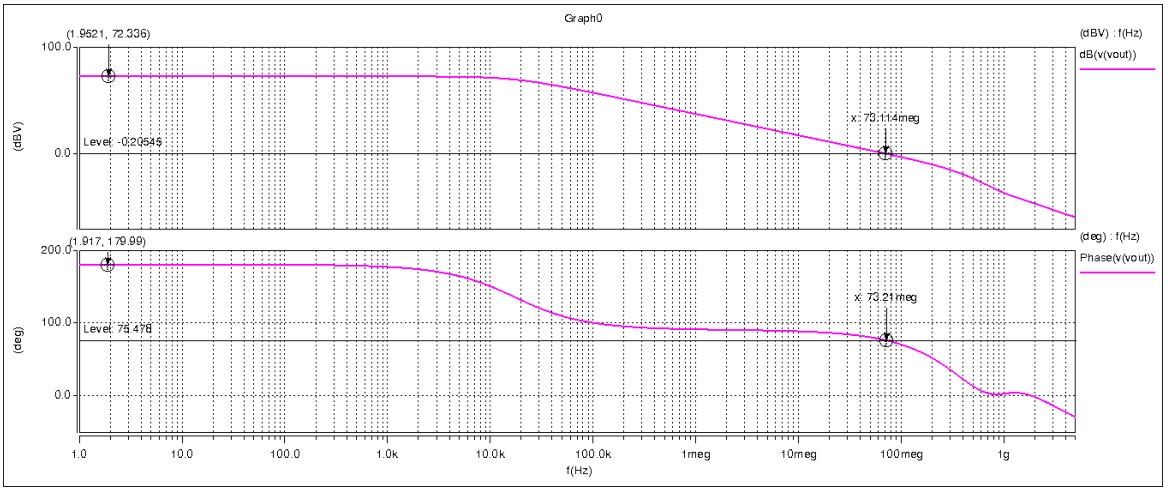

Fig. 7. (a) Frequency response of the gain of the recycling feedback amplifier (RFC), (b) Phase margin of the operational transconductance amplifier

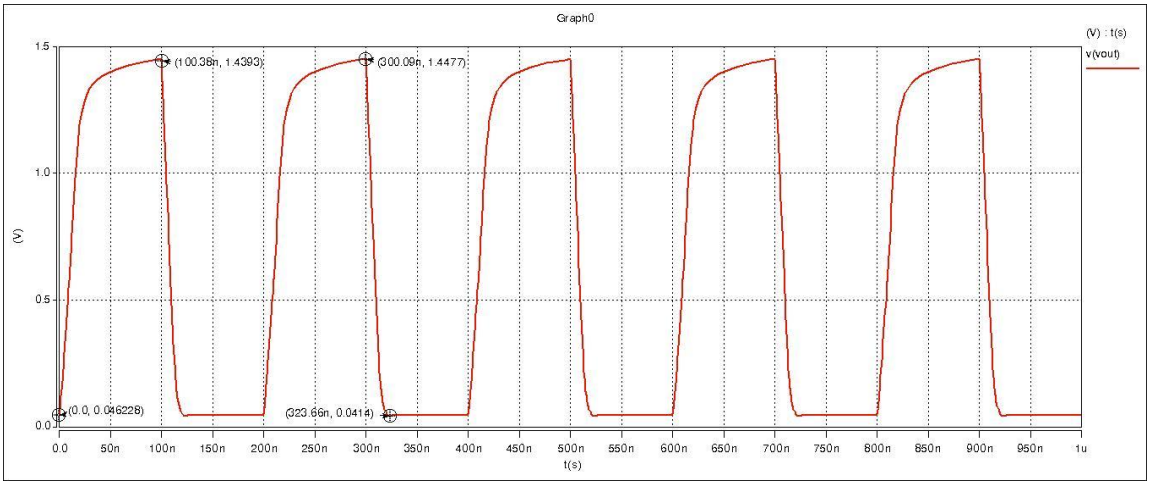

Fig. 8. Slew rate of the operational transconductance amplifier

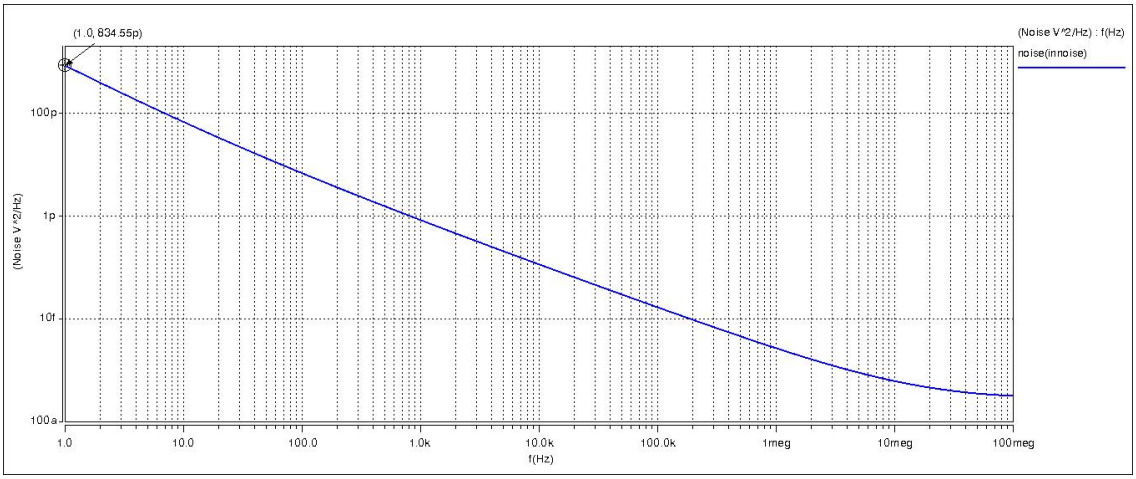

Fig. 9. Input noise of the operational transconductance amplifier

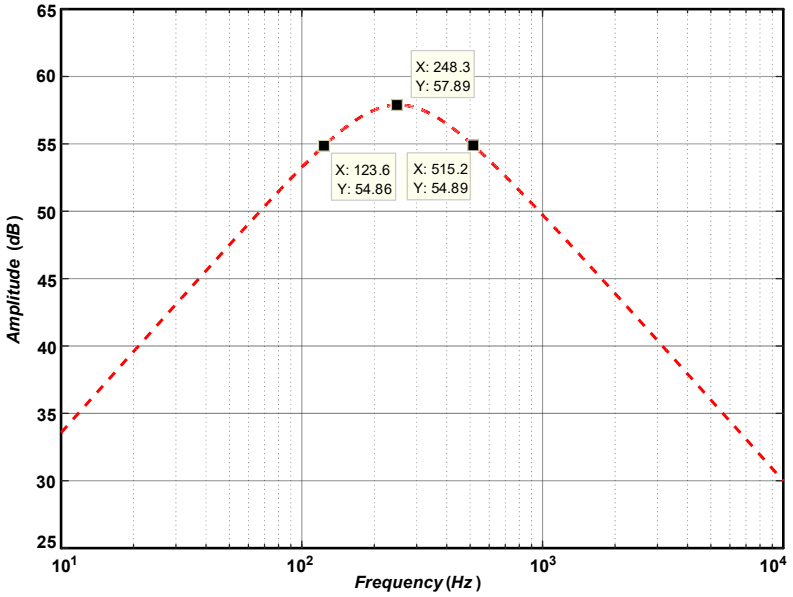

Fig. 10. The frequency response of the gain of the preamplifier stage.

Table 3 summarizes the simulation results of the operational transconductance amplifier. As observed in Figure 10, the output of the preamplifier is close to the range of the brain signal; however, since the desired information in the signal is hidden in a specific range, this range should be selected using a bandpass filter from the entire frequency range, and the other components outside this band should be filtered. In the next section, you will see the simulation results of the selected bandpass filter.

Table 3. Target Specifications for the Design of the Operational Transconductance Amplifier

Parameters	**TT @ 27 ℃**	**Parameters**	**TT @ 27 ℃**
Power dissipation (μW)	165 · 1	DC Gain (dB)	**72 · 27**
BW (KHz)	20	GBW (MHz)	**71 · 92**
slew rate (v/ns)	100	Open Loop PM (deg)	**75 · 80**
CMRR (dB)	128	Capacitive Load (pF)	**1**
PSRR (dB)	103	Input referred noise [1 Hz – 100 MHz] (μV_{rms})	**237 · 6**

5. CONCLUSION

In this article, we have designed an integrated pre-amplifier for recording neural signals. The most critical features of this system are its power consumption and noise. The power consumption of the μv48 pre-amplifier and the reference noise of the amplifier are 260 $\frac{\mathbf{V^2}}{\mathbf{Hz}}$, respectively. Additionally, one of the most significant challenges in the design of the pre-amplifier was achieving frequencies below 1 kHz, which was resolved using a pseudo-resistance. This pseudo-resistance provides a resistance of 7.95 GΩ, which, combined with a 0.1PF capacitor, can create a lower cutoff frequency of 150 Hz, which is crucial for the reception of neural signals.

Furthermore, by considering appropriate values for the bias current and Gm, the load capacitance CL, and the mid-band gain, we have tuned the upper cutoff frequency of the pre-amplifier, such that the lower and upper cutoff frequencies are 150 Hz and 520 Hz, respectively. Consequently, the brain signal is between μv80 and mv2. Therefore, the gain should be appropriately adjusted to accommodate the amplitude variations of the signal. In this article, the pre-amplifier gain is around 40 dB, and the RFC amplifier gain used in the pre-amplifier structure is 72.27 dB.

The designed amplifier has the capability to be integrated into a medical chip, and by placing it alongside a band-pass filter and an ADC with appropriate resolution, it can enable the digital acquisition of information.

Transparency Statement

The data supporting this study are available upon reasonable request to the corresponding author, subject to ethical and confidentiality considerations.

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Declaration of Interest

The authors declare that they have no competing interests.

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