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Design of a Low-Power and Low-Noise Neural Recording Front-End Block for Seizure Detection

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ABSTRACT

The design of a dedicated block within an epilepsy seizure detection system, intended for both medical and localized applications, plays a crucial role in amplifying vital and neural signals from the body, particularly brain and heart signals, thereby assisting in the precise diagnosis of various disease types. This paper focuses on the design and development of the front-end circuit of neural signal recording systems, which primarily consists of an amplifier and a bandpass filter. A key objective in this design is achieving low power consumption and minimal noise while maintaining high performance. To accomplish this, an amplifier with an RFC (resistor-feedback capacitor) structure is selected, offering the advantage of delivering high gain and reduced noise at comparable power levels. Furthermore, by employing an elliptic bandpass filter configured as a Gm-C (transconductance-capacitor) filter, the system effectively addresses the challenges posed by signal ripple, resulting in enhanced signal quality, lower power usage, minimized noise, and a smaller circuit footprint. The proposed design is implemented using 180 nm CMOS technology, leveraging the TSMC BSIM library, and simulations are conducted using HSPICE 2008 software to validate the system's performance. This work contributes valuable insights for developing efficient, compact, and reliable neural signal processing modules for biomedical applications.

1. INTRODUCTION

Approximately 50 million individuals worldwide suffer from epilepsy, and about one-third of them experience seizures that are refractory to pharmacological treatment. Brain stimulation can be an effective approach for controlling intractable epileptic seizures [1-4]. One of the challenges in brain stimulation-based treatment is the accurate detection of seizure onset and occurrence. Recently, researchers have been attempting to design and implement an implantable deep brain stimulation chip with the capability of automated brain activity detection [5]. Mounting evidence suggests that the occurrence of a specific type of high-frequency oscillations in the brain activity

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of epilepsy patients is closely associated with the onset of seizures. This signal can be recorded using the IEEG method and can provide valuable information for detecting the timing of seizure occurrence. The signal energy is predominantly within the 200 to 600 Hz frequency range, and the amplitude ranges from 30 µV to 1.5 mV, depending on the size of the electrodes used in the IEEG recording process [6].

Since seizures can occur at any time, the intended integrated circuit must perform continuous signal recording for an extended period, necessitating the requirement of low power consumption. Additionally, the neural signal recording circuit must effectively amplify the weak input signals before any further processing. Furthermore, given the small amplitude of the recorded neural signals, the input-referred noise of the entire system must be very low to ensure the integrity of the signal recording process. Therefore, this work focuses on the design of a low-power, low-noise front-end circuit for the brain signal recording system.

2. OVERALL SYSTEM STRUCTURE

Based on the structure shown in Figure 1, the front-end circuit of the targeted brain signal recording system consists of two stages. The initial stage includes a preamplifier circuit to increase the amplitude of the weak recorded signals and prepare them for further processing. The subsequent stage is a bandpass filter to select the specific frequency range where the energy of the FR signal is concentrated [5-7].

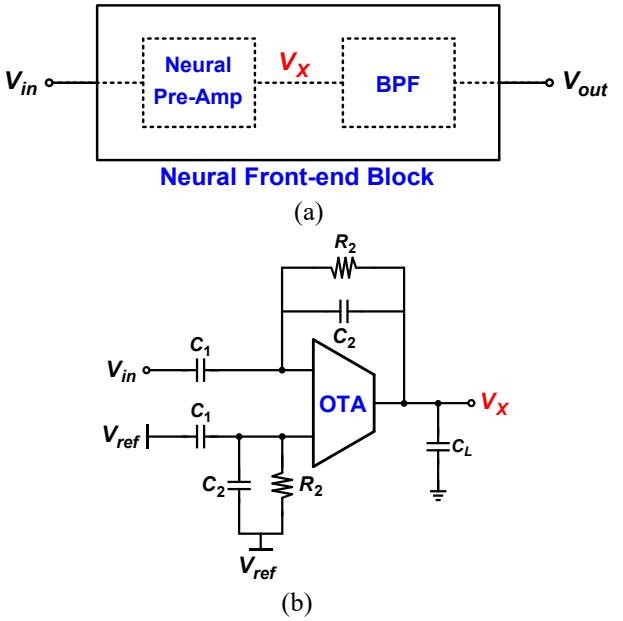

Fig. 1. (a) Structure of the front-end stage of the neural signal recording system, (b) Structure of the neural signal preamplifier circuit

2.1. Preamplifier stage

The targeted preamplifier stage is based on an operational transconductance amplifier (OTA) with a capacitive feedback structure, as shown in Figure 1. This OTA-based preamplifier generates an output current proportional to the input voltage difference, where Gm is the constant of this proportionality. The midband gain (Am) of the amplifier is determined by the ratio of C1/C2, and its bandwidth is approximately Gm(AmCL) for $C1 \cdot CL \gg C2$. The recorded signal is coupled to the circuit through the capacitor C1, which eliminates the DC offset generated at the electrode-tissue interface and allows only the AC component of the recorded signal to be amplified, thus preventing the amplifier from saturation due to the high gain required for the weak recorded signals [7-8].

The feedback resistor R2 sets the lower cutoff frequency of the preamplifier. These resistors are implemented on-chip using pseudo-resistors, which are realized using PMOS and NMOS transistors [9].

The input-output transfer function of the preamplifier stage is given by:

$$\frac{V_X}{V_{in}} = \frac{C_1}{C_2} \cdot \frac{\frac{1-sC_2}{G_m}}{\left(\frac{1}{sR_2C_2}+1\right)\left(s\frac{C_LC_1}{G_mC_2}+1\right)} = A_M \frac{1-s/(2\pi f_Z)}{\left(1+\frac{2\pi f_L}{s}\right)\left(1+\frac{s}{2\pi f_H}\right)} \quad (1)$$

According to Equation (1), the midband gain Am is determined by the C1/C2 ratio, and the gain between the lower and upper cutoff frequencies is flat. The lower cutoff frequency is set by the R2 and C2 combination. The upper cutoff frequency is determined by the load capacitance CL, the OTA transconductance, and the midband gain. The capacitive feedback introduces a positive zero at the frequency fz, which can be shifted to very high frequencies by choosing C2 ≪ √(C1CL). Figure 2 shows the frequency response of the preamplifier circuit [10].

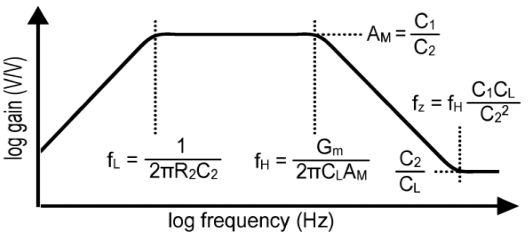

Fig. 2. The frequency response of the gain of the pre-amplifier circuit.

Figure 3 illustrates the placement of the existing noise sources in the pre-amplifier circuit. Figure 4 shows the different components of the overall output noise of the amplifier in a case where both noise sources V_{nia} and V_{nR} are white noise. The OTA noise is predominantly located in the range between the lower and upper cutoff frequencies. The noise from V_{nR} also dominates for frequencies lower than the corner frequency f_{corner}.

If the resistance R2 is implemented using a real resistor, its noise power spectral density is given by:

$$v_{nR}^2(f) = 4kTR_2 \quad (2)$$

If C1 ≫ C2, Cin, the corner frequency is approximately:

$$f_{corner} \approx \sqrt{\frac{3C_L}{2C_1} f_L f_H} \quad (3)$$

To reduce the noise from R2, the corner frequency must be much lower than the upper cutoff frequency of the entire circuit. For this purpose, the amplifier must be designed such that the following condition is met:

$$\frac{C_L}{C_1} \ll \frac{2f_H}{3f_L} \quad (4)$$

If the noise from the R2 resistance is negligible, i.e., $f_{corner} \ll f_H$ and $C_1 \gg C_2$, C_{in}, then the rms output noise voltage of the amplifier in Figure 4 is limited to the noise from the OTA.

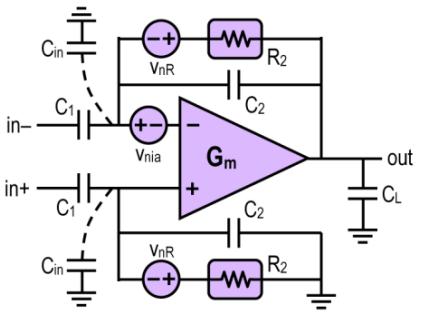

Fig. 3. Noise source modeling of the preamplifier circuit

The input-referred thermal noise power spectral density of the OTA is given by:

$$v_{nia}^2(f) = \frac{16kT}{3g_{m1}}\left(1 + 2\frac{g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right) \quad (5)$$

where gm1 is the transconductance of transistors M1,2, gm3 is the transconductance of transistors M(3-6), and gm7 is the transconductance related to transistors M7,8.

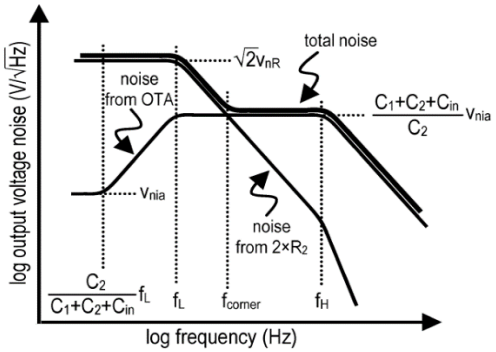

Fig. 4. Output noise of the preamplifier circuit as a function of frequency

2.1.1. Structure selection for the OTA

The Folded Cascode (FC) amplifier has become one of the most widely used structures, both as a single-stage and as the first stage in multi-stage low-voltage CMOS processes, due to its high voltage gain and large signal swing. Furthermore, the FC with a PMOS input has much greater application than the FC with an NMOS input, due to its higher non-dominant pole, lower flicker noise, and better common-mode input level. In switched-capacitor circuits, the input switching operation can be performed using a single NMOS transistor.

The conventional FC amplifier is shown in Figure 5. Note that transistors M3 and M4 carry the largest currents and, in many designs, have the highest transconductance. However, their function is to provide a Folding node for the small signal currents generated by the input drivers (M1 and M2). To this end, the modified Folded Cascode structure shown in Figure 6 has been designed. In this structure, transistors M3 and M4 are used as the driver transistors. First, the input drivers (M1 and M2) in Figure 5 are replaced by transistors M1a, M1b, M2a, and M2b in Figure 6. These transistors carry a fixed and equal current (Ib/2). Transistors M3 and M4 in Figure 5 are also replaced by transistors M3a, M3b, M4a, and M4b in Figure 6 to form two current mirrors with a K:1 ratio. The cross-connection of these two current sources ensures that the small signal currents added at the sources of M5 and M6 are in-phase. Finally, transistors M11 and M12 are sized similarly to M5 and M6, and their use ensures that the drain potentials of M3a, M3b, M4a, and M4b are equal, resulting in better matching [10-14].

2.1.2. Recycled Folded Cascode (RFC)

To provide qualitative evidence of the improvements in the RFC structure, it has been assumed that all transistors operate in the saturation region.

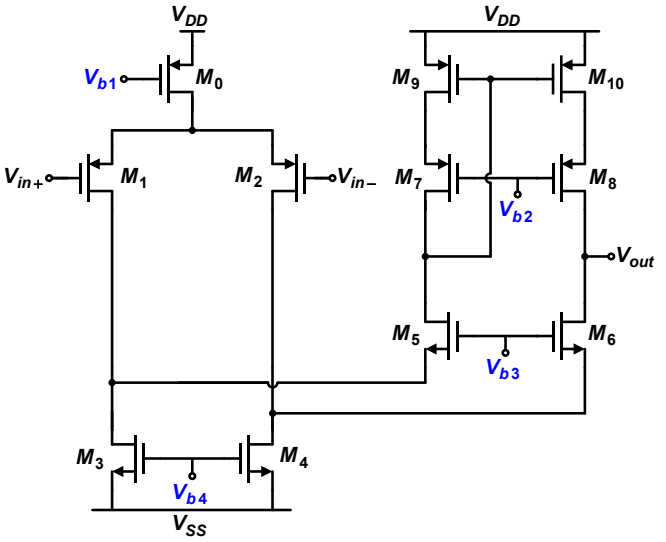

Fig. 5. Conventional Recycled Cascode Amplifier

Additionally, the current gain K is chosen to be 3. This ensures that the power consumption is identical for the FC and RFC structures. It should be noted that the current flowing through transistors M5 to M10 is a function of K. For K≠3, the transistors M5 to M10 must be rescaled to achieve the same power consumption and area as the FC circuit in the case of K=3.

The analyses presented hereafter are valid for both the single-ended and differential amplifier configurations. However, the discussion focuses primarily on the fully differential structure.

2.1.3. Small-Signal Transconductance

The amplifier transconductance, Gm, can be found using the ratio of the output short-circuit current to the input. The desired results for the RFC and FC structures are shown in equations (6) and (7), respectively:

$$G_{m.RFC} = g_{m1a}(1 + K) \tag{6}$$

$$G_{m.FC} = g_{m1} \tag{7}$$

Considering that the size of M1 is twice the size of M1a and it also draws twice the current ($g_{m1}=2g_{m1a}$), and substituting the value of K, it can be concluded that the RFC transconductance is twice the FC transconductance for the same power consumption. In other words, for the same power consumption, the gain-bandwidth product (GBW) of the RFC is approximately twice that of the FC structure, and consequently, it has twice the speed [12, 13].

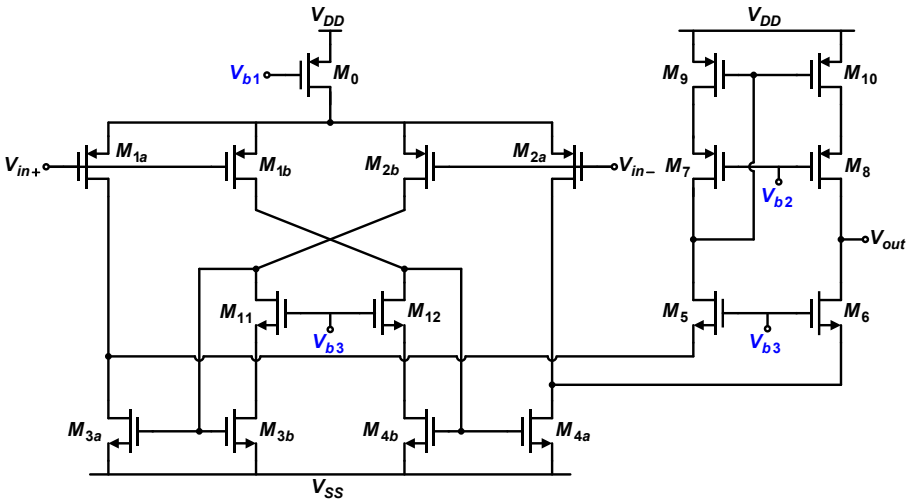

Fig. 6. RFC Amplifier

Additionally, the bias circuit for the Recycled Cascode (RFC) amplifier to provide the desired operating points is shown in Figure 7.

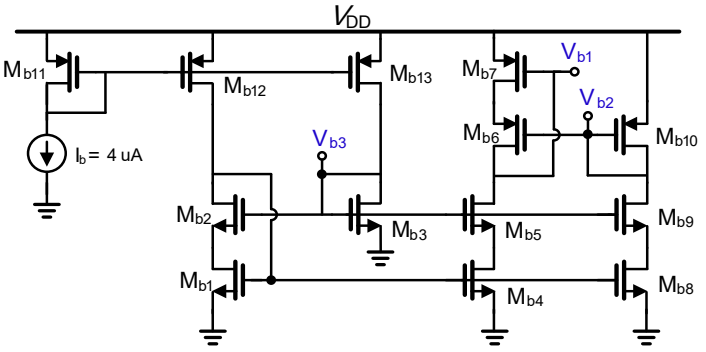

Fig. 7. RFC Biasing Circuit

2.1.4. Low Frequency Gain

The low-frequency gain of OTAs is generally expressed as the product of the small-signal transconductance Gm and the low-frequency output impedance, Ro. It has been shown that (Gm.RFC =2Gm.FC), which results in a 6 dB gain improvement for the same output impedance. However, the output impedance of the RFC has been significantly improved compared to the FC, as observed in the following relationships:

$$Ro_{FC} \cong g_{m6} r_{ds6} (r_{ds2} \| r_{ds4}) \| g_{m8} r_{ds8} r_{ds10} \quad (8)$$

$$Ro_{RFC} \cong g_{m6} r_{ds6} (r_{ds2a} \| r_{ds4a}) \| g_{m8} r_{ds8} r_{ds10} \quad (9)$$

The increase in the gain due to the higher output impedance of the RFC structure is attributed to the increase in the r_{ds} of transistors M_{2a} and M_{4a}, implying that these transistors draw less current compared to their counterparts (M_2 and M_4) in the FC structure. Consequently, the overall low-frequency gain exhibits an 8-10 dB improvement over the FC structure.

This additional gain has two significant advantages. First, it reduces the static offset errors due to the increased gain. Secondly, the PSRR of the RFC is improved compared to the FC structure. The PSRR is equal to the ratio of the gain of the noise injected from the power supply to the gain of the input signal. Both the RFC and FC structures have the same gain of the injected noise, but the loop gain of the RFC is higher, resulting in better PSRR performance.

Furthermore, the increased GBW of the RFC structure also provides improved PSRR performance at higher frequencies compared to the FC structure [11-14].

2.1.5. Slew Rate

The slew rate is obtained from the derivative of the maximum output current that charges the load capacitor. It is obtained such that if a large voltage is applied to the input V (in+), Mb1 and Ma1 turn off, which in turn causes Ma4 and Mb4 to turn off as well, and their drain voltages rise, leading to the turning off of M6 and the placement of Ma2 in the deep ohmic region. Consequently, the current of Mb2 is transferred to the output through the gains K and K-1, and the slew rates for the RFC and FC amplifiers are respectively defined in 10 and 11 [13].

$$S.R_{RFC} = \frac{2KI}{C_L} \tag{10}$$

$$SR_{FC} = \frac{2I}{C_L} \tag{11}$$

2.1.6. Phase Margin

To have a suitable phase margin, one must pay attention to the location of the zeros and poles of the RFC amplifier. The first pole is related to the output impedance and capacitance, the second pole is related to the source of transistors M5 and M6, and the third pole is related to the gate of the current mirror transistors. Opposing this, a mirror zero with a value of K+1 times the mirror pole also appears. To have a suitable phase margin from this amplifier, the third pole should be sufficiently far from the unity gain frequency, i.e.:

$$|\omega_{P3}| \geq |3\omega_{GBW}| \rightarrow K \leq \sqrt{\frac{C_L g_{mb3}}{3 g_{ma1} C_{gsb3}}} - 1 \tag{12}$$

Where ωP3 is the third pole and ωGBW is the unity gain frequency of the amplifier. Also, gmb3 and Cgsb3 are the transconductance and gate-source capacitance of transistor Mb3, respectively [12].

2.1.7. Noise

In many applications such as audio amplifiers, continuous-time filters, and data converters, noise can be a limiting factor in the design. The maximum noise current power seen at the output of a MOSFET is given by:

$$\overline{i_o^2} = \left[4k_B T\gamma gm + \frac{K_F I_D}{C_{ox} L^2 f}\right].\Delta f \tag{13}$$

Where the first and second terms represent the thermal noise and flicker noise, respectively. For comparison, the thermal and flicker noise components have been examined separately. The referred-to-input thermal noise for the FC and RFC amplifiers is respectively given by:

$$\overline{v_{iT.FC}^2} = \frac{8k_B T\gamma}{gm_1}\left[1 + \frac{gm_3}{gm_1} + \frac{gm_9}{gm_1}\right].\Delta f \tag{14}$$

$$\overline{v_{iT.RFC}^2} = \frac{8k_B T\gamma}{gm_{1a}}\left[\frac{(1+K^2)}{(1+K)} + \frac{gm_{3a}}{gm_{1a}} + \frac{1}{(1+K)}\frac{gm_9}{gm_{1a}}\right].\Delta f \tag{15}$$

By replacing gm1a with gm1 and gm3a in the expressions for gm3, and also substituting the value of K, equation (16) is transformed into the following relation:

$$\overline{V_{iT.RFC}^2} = \frac{8k_B T\gamma}{gm_1}\left[\frac{5}{4} + \frac{3gm_3}{4gm_1} + \frac{1}{4}\frac{gm_9}{gm_1}\right].\Delta f \tag{16}$$

The flicker noise associated with the FC and RFC structures is respectively expressed by the following equations:

$$\overline{v_{if.FC}^2} = \frac{K_{FP}}{\mu_p C_{ox}^2 W_1 L_1 f}\left[1 + 2\frac{K_{FN}}{K_{FP}} + \left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_9}\right)^2\right].\Delta f \quad (17)$$

$$\overline{v_{if.RFC}^2} = \frac{K_{FP}}{\mu_p C_{ox}^2 W_{1a} L_{1a}(1+K) f}\left[\frac{(1+K^2)}{(1+K)} + K\frac{K_{FN}}{K_{FP}} + \left(\frac{L_{1a}}{L_{3a}}\right)^2 + \frac{(K-1)}{(1+K)}\left(\frac{L_{1a}}{L_9}\right)^2\right] \quad (18)$$

The modifications made to the FC structure to obtain the RFC structure only relate to the width of the transistors, and no changes were made to the length of the transistors. Therefore, by replacing W1a with expressions of W1 and also substituting the value of K, the following equation is obtained for $\overline{v_{if.RFC}^2}$:

$$\overline{v_{if.RFC}^2} = \frac{K_{FP}}{\mu_p C_{ox}^2 W_1 L_1 f}\left[\frac{5}{4} + 1.5\frac{K_{FN}}{K_{FP}} + \left(\frac{L_1}{L_3}\right)^2 + \frac{1}{4}\left(\frac{L_1}{L_9}\right)^2\right].\Delta f \quad (19)$$

Considering the above equations, since two terms in $\overline{v_{if.RFC}^2}$ and $\overline{v_{iT.RFC}^2}$ are smaller than their counterparts in $\overline{v_{if.FC}^2}$ and $\overline{v_{iT.FC}^2}$, it can be concluded that the RFC structure has lower noise compared to the FC structure.

2.1.8. Calculation of the Preamplifier Capacitor and Resistor

After designing the required OTA (Operational Transconductance Amplifier) used in the structure of the preamplifier stage, it is time to design the entire section and determine the values of the capacitors and resistors used to achieve the desired specifications, as outlined in Table 1.

Table 1. Specifications of the Preamplifier

Parameter	Value
Gain	**≥ 40 dB**
Bandwidth	**200 Hz − 600 Hz**
C_L	**1 pF**

To achieve the specified low cutoff frequency, the values of resistance R2 and capacitor C2 need to be calculated according to the following relationship:

$$F_L = \frac{1}{2\pi R_2 C_2} \xrightarrow{(f_L=200\ Hz)} 200 = \frac{1}{2\pi R_2 C_2} \xrightarrow{C_2=0.1\ pF} R_2 = \frac{1}{2\pi\times 200\times 0.1\ pF} = 7.95\ G\Omega \quad (20)$$

As observed, the value of resistance R2 is very large and needs to be implemented within the integrated circuit. The dimensions of the transistors forming the pseudo-resistance R2 to achieve a resistance of 7.95 GΩ are provided in Table 3.

For the pre-amplifier circuit, considering the relationship (1) to achieve a gain greater than 40 dB and the potential attenuation of the overall gain in the bandpass filter, the value of capacitor C1 needs to be designed according to the following relationship (22) to meet the above conditions:

$$A_M = \frac{C_1}{C_2} \xrightarrow{(A_M\geq 40\ dB)} 10^{\frac{60}{20}} = \frac{C_1}{0.1\ pF} \xrightarrow{C_2=0.1\ pF} 10^3 = \frac{C_1}{0.1\ pF} = 100\ pF \quad (21)$$

Additionally, the upper cutoff frequency of the pre-amplifier circuit can be obtained from the relationship (22), which depends on the load capacitance CL, the amplifier transconductance Gm, and the mid-band gain Am.

$$f_H = \frac{G_m}{2\pi C_L A_M} \quad (22)$$

2.2 Design of the Band-Pass Filter

After designing the pre-amplifier stage to increase the amplitude of the recorded weak signals, and given that the desired information is embedded within a specific frequency range in the FR signal, it is necessary to select this frequency range using a band-pass filter from the entire frequency spectrum, and filter out the components outside this band. To this end, the output of the pre-amplifier stage is connected to a band-pass filter, and the useful information in the FR signal is extracted.

Since the frequency range was already selected using the resistance and capacitance structure in the pre-amplifier stage, the selected band-pass filter is a Gm-C filter, as shown in Figure 11. In the following, a 6th-order Gm-C band-pass filter with a passband of 200 Hz to 600 Hz is designed and simulated to extract the useful information from the FR signal.

2.2.1. General Structure of Gm-C Filters

The Gm-C filter consists of two main blocks: the transconductance block (Gm) and the capacitor (C). In the transconductance block, the output current (Iout) is a function of the input voltage difference, i.e., Iout = Gm(Vin+ - Vin-), where Gm is the transconductance of the amplifier block.

2.2.2. Design and Implementation of a 6th-Order Gm-C Band-Pass Filter

The block diagram shown in Figure 8 represents the implementation of a 6th-order Gm-C band-pass filter. It is evident that a second-order band-pass filter must have one zero and two poles, and under specific conditions, the locations of these zero and poles determine the passband bandwidth of the filter.

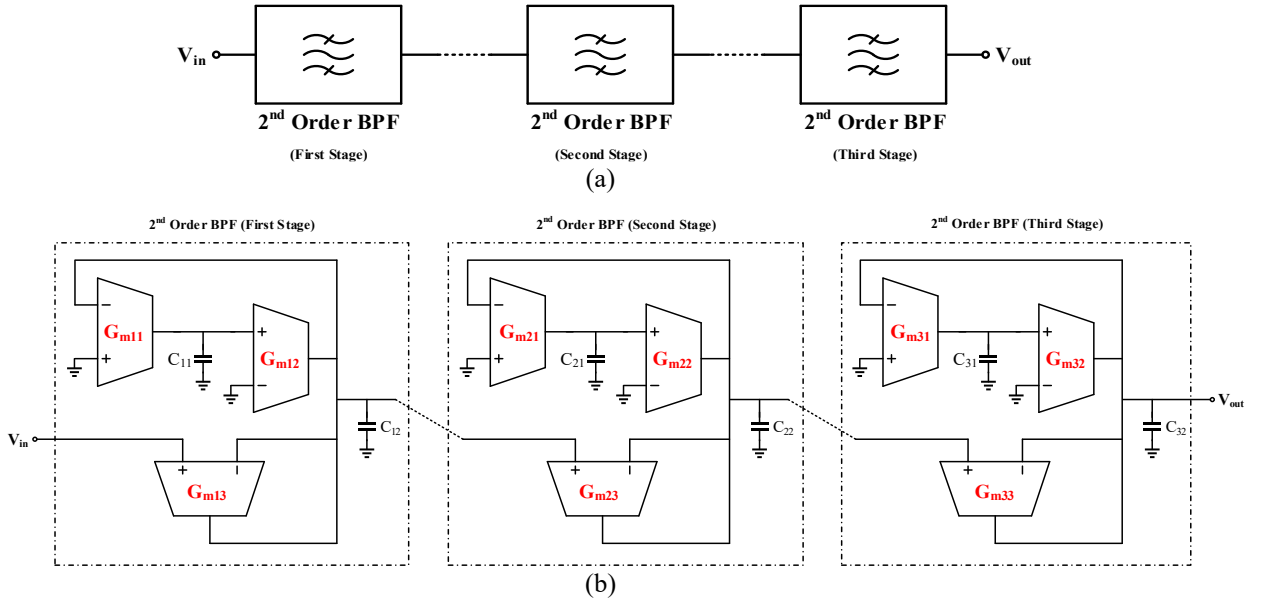

Fig. 8. (a) Block diagram of a 6th order low-pass filter, (b) Circuit implementation of a 6th order low-pass filter.

Considering Figure 8 and writing the governing circuit relationships of the given structure, the transfer function between the input and output of the filter can be obtained. In fact, based on the location of the zeros and poles of this relationship, it is well-proven that the given structure has the capability to implement a low-pass filter.

$$TF_{BP} = \frac{V_{out}}{V_{in}} = \frac{s\left(\frac{G_{m3}}{C_2}\right)}{s^2 + s\left(\frac{G_{m3}}{C_2}\right) + \frac{G_{m1}G_{m2}}{C_1C_2}} \tag{23}$$

Given the above transfer function, the center frequency ω0 and the quality factor Q of the circuit can be adjusted by varying the circuit parameters according to the following relationships:

$$\omega_0 = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} \tag{24}$$

$$Q = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}} \times \frac{C_2}{G_{m3}} \tag{25}$$

Therefore, assuming the transconductance Gm of all the transconductance amplifiers is constant, one can readily tune the center frequency and the desired bandwidth of the 2nd-order low-pass filter by varying the capacitor values C1 and C2. The following formula shows the relationship between the center frequency, quality factor, and bandwidth:

$$BW = \frac{f_0}{Q} \Rightarrow BW \propto \frac{G_{m3}}{C_2} \tag{26}$$

From the above relationship, it can be concluded that, for a constant Gm of all the transconductance amplifiers, in order to increase the passband bandwidth of the low-pass filter, the capacitor C2 should be decreased, which in turn increases the center frequency ω0. Therefore, to increase the passband bandwidth while keeping the center frequency ω0 constant, the capacitor C2 should be decreased, and the capacitor C1 should be increased simultaneously. The internal structure of the designed OTA block is shown in Figure 9. The transistor dimensions and their bias currents can be adjusted according to the required specifications for the desired filter design.

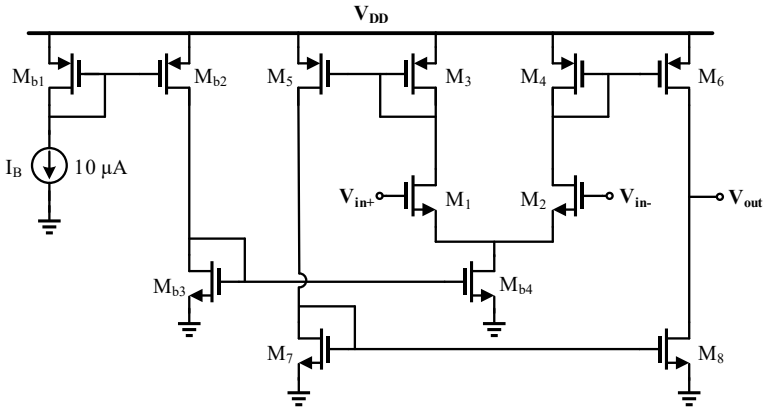

Fig. 9. Internal Structure of the Transconductance Operational Amplifier Circuit for the Gm Cell

The gain Gm of the amplifier in our design is 65 $\frac{\mu A}{V}$. To achieve a 6th-order lowpass filter, three 2nd-order lowpass filter stages can be cascaded in series.

It should be noted that all stages have the same center frequency and passband bandwidth, and the circuit elements in each of the three stages are identical. By substituting the circuit elements, the overall structure of the 6th-order lowpass filter is revealed. The capacitor values used in the above structure to achieve the desired center frequency and bandwidth are summarized in Table 4.

3. SIMULATION RESULTS

As explained, the neural signal acquisition system consists of a preamplifier and a lowpass filter, with a transimpedance amplifier as the core of both subsections. This section presents the simulation results in three stages: 1) preamplifier simulation results, 2) lowpass filter simulation results, and 3) overall neural signal acquisition system simulation results.

3.1. Preamplifier Simulation Results

This amplifier is designed in TSMC's 180 nm technology with a gain of 27.72 dB. The frequency response of the input-output gain of the designed feedback-based amplifier is shown in Figure 10. The transistor dimensions and the biasing design for the amplifier are provided in Table 2. For the amplifier, the phase margin is 80.75 degrees, the rising-edge slew rate is 100 V/ns, and the falling-edge slew rate is 26 V/ns, as shown in Figure 11. Figure 12 shows the input-referred noise spectrum, with a total input-referred noise of 260 $\frac{V^2}{Hz}$.

Table 2. Transistor dimensions and biasing for the amplifier circuit

Main OTA											
M	W (µm) /L (µm)	Tr.	M	W (µm) /L (µm)	Tr.	M	W (µm) /L (µm)	Tr.	M	W (µm) /L (µm)	**Tr.**
1	0.3/3	$M_{3b.4b}$	4	0.46/0.36	$M_{11.12}$	2	0.66/0.36	$M_{1a.2a}$	4	1.25/0.36	$\mathbf{M_0}$
8	0.46/0.36	$M_{5.6}$	16	0.36/0.36	$M_{7.8}$	1	0.3/0.9	$M_{3a.4a}$	2	0.72/0.36	$\mathbf{M_{1b.2b}}$
									8	0.34/0.36	$\mathbf{M_{9.10}}$
Bias Circuit											
M	W (µm) /L (µm)	Tr.	M	W (µm) /L (µm)	Tr.	M	W (µm) /L (µm)	Tr.	M	W (µm)/L (µm)	**Tr.**
2	0.34/0.72	M_{b10}	4	0.29/0.36	M_{b13}	4	0.46/0.36	M_{b2}	1	0.3/3	$\mathbf{M_{b1}}$
4	0.52/0.36	M_{b9}	2	0.32/0.36	M_{b11}	1	0.3/3	M_{b4}	1	0.27/3	$\mathbf{M_{b3}}$
1	0.3/3	M_{b8}	2	0.32/0.36	M_{b12}	2	0.52/0.18	M_{b6}	4	0.46/0.36	$\mathbf{M_{b5}}$
									1	0.53/0.18	$\mathbf{M_{b7}}$

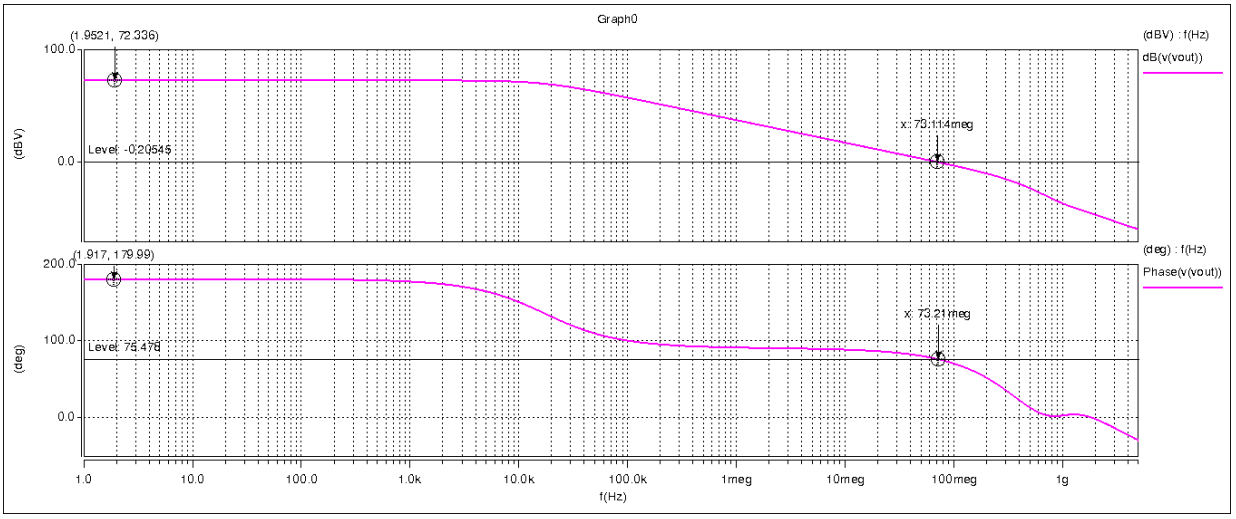

Fig. 10. (a) Frequency Response of the Gain of the Recycled Folded Cascode (RFC) Amplifier, (b) Phase Margin of the Transconductance Operational Amplifier

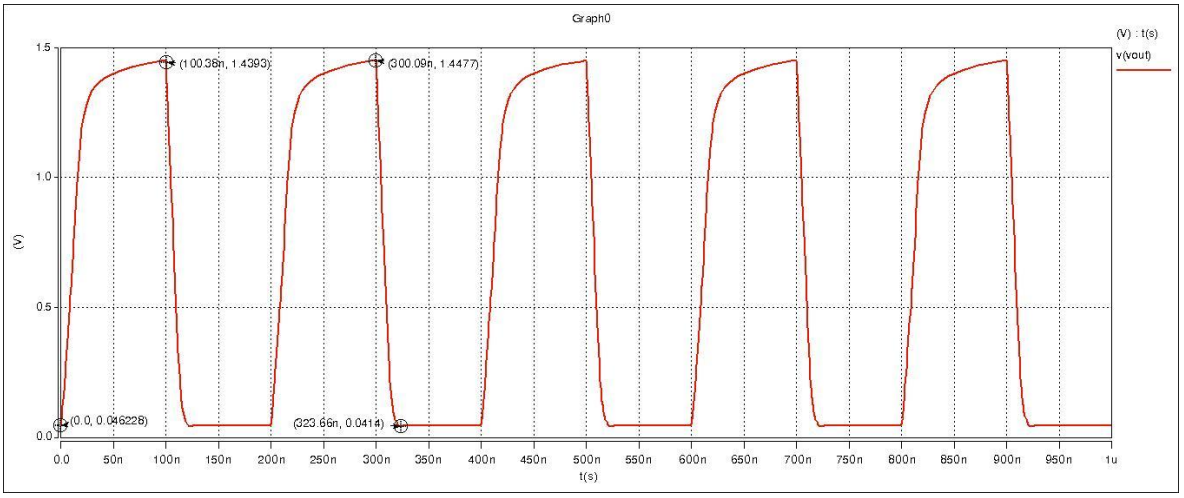

Fig. 11. Slew Rate of the Transconductance Operational Amplifier

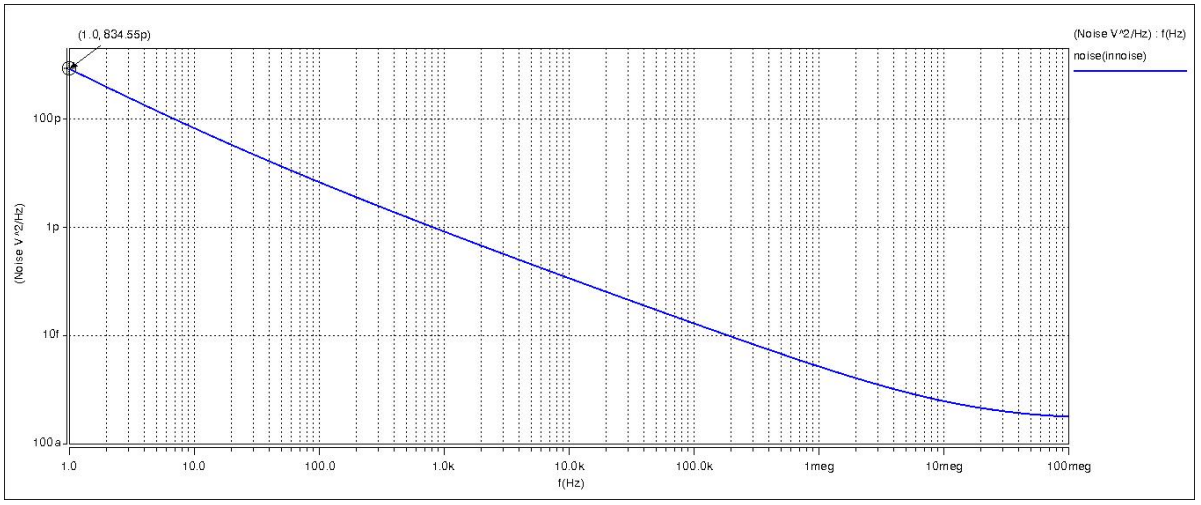

Fig. 12. Input-referred noise of the transimpedance operational amplifier

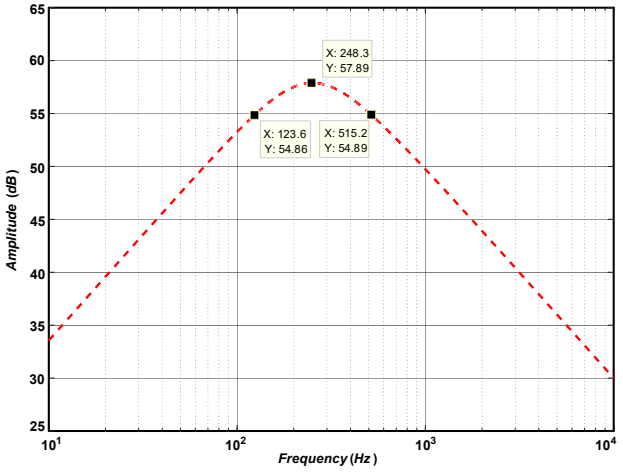

Fig. 13. Frequency response of the gain for the pre-amplifier stage

Table 3 summarizes the simulation results of the transimpedance amplifier design. As observed in Figure 13, the output of the pre-amplifier stage is approximately within the range of the brain signal. However, since the information of interest in the signal is confined to a specific frequency range, this band must be selected by a bandpass filter from the entire frequency spectrum, and the other components outside this band must be filtered out. In the next section, you will see the simulation results of the selected bandpass filter.

Table 3. Target specifications for the design of the transimpedance operational amplifier

Parameters	**TT @ 27 ℃**	**Parameters**	**TT @ 27 ℃**
Power dissipation (μW)	$165 \cdot 1$	DC Gain (dB)	$\mathbf{72 \cdot 27}$
BW (KHz)	20	GBW (MHz)	$\mathbf{71 \cdot 92}$
slew rate (v/ns)	100	Open Loop PM (deg)	$\mathbf{75 \cdot 80}$
CMRR (dB)	128	Capacitive Load (pF)	**1**
PSRR (dB)	103	Input referred noise $[1\ \mathrm{Hz} - 100\ \mathrm{MHz}]$ (μV_{rms})	$\mathbf{237 \cdot 6}$

The bandpass filter was designed in the 180nm CMOS technology from TSMC. It is composed of three cascaded second-order bandpass filters. Each second-order filter stage has three Gm cells and two capacitors C1 and C2, where the required Gm value is obtained from the previously designed transimpedance amplifier.

The transimpedance amplifier was designed with a gain of 26 dB and an impedance of 311 kΩ. The values of the capacitors used in the filter structure were chosen to achieve the desired center frequency and bandwidth.

Table 4 summarizes the off-chip capacitor values and the overall specifications of the 6th-order bandpass filter:

Table 4. Off-chip Capacitor Values and 6th-Order Bandpass Filter Specifications

	Theory	**Simulation**	**Theory**		**Simulation**	**Theory**		**Simulation**
$C_{11.21.31}$	31 nF	60 nF	f_0	350 Hz	385 Hz	f_H	600 Hz	**635 Hz**
$C_{12.22.32}$	24 nF	12 nF	f_L	200 Hz	228 Hz	Q	0.875	**0.946**

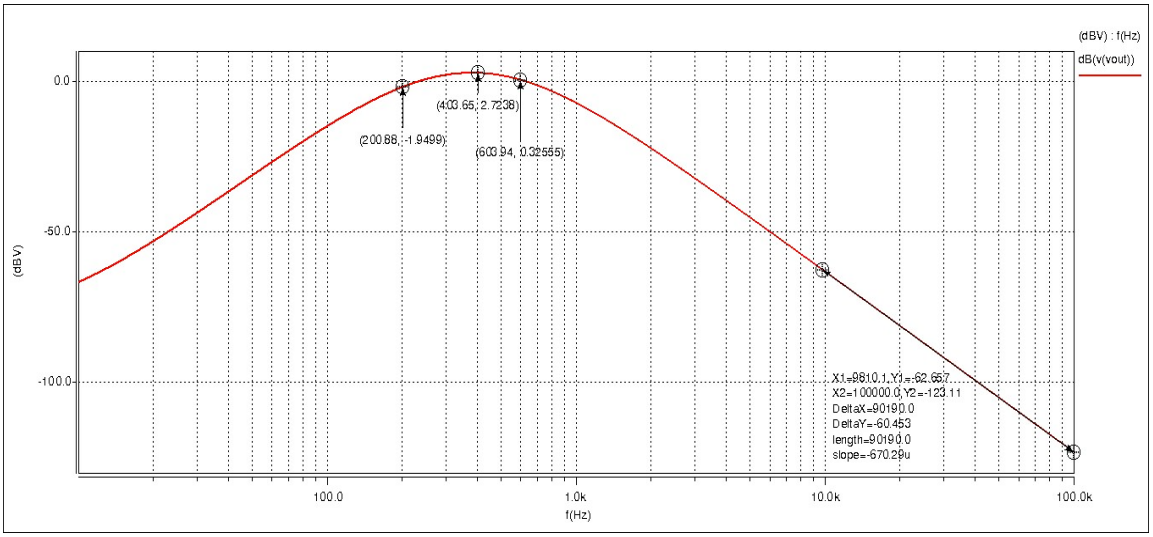

Fig. 14. Frequency Response of the Output (6th-Order Bandpass Filter)

3.2. Simulation Results of the Front-End Neural Signal Recording System

Now, if the designed 6th-order bandpass filter is placed after the amplifier block, the frequency response of the amplifier's gain for the brain signal will be as depicted in the figure below.

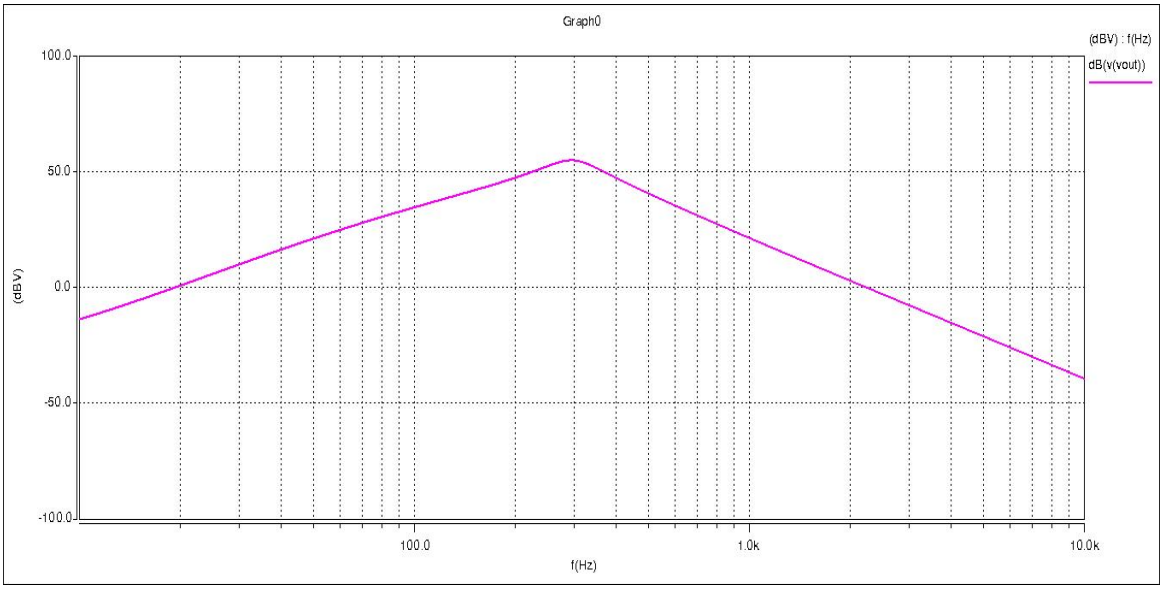

Fig. 15. Frequency response of the gain of the front-end system for neural signal recording

4. CONCLUSION

In this paper, we have designed an integrated front-end circuit for a neural signal recording system, comprising an amplifier and a bandpass filter. The most critical characteristics of this system are its power consumption and noise performance. The power consumption of the preamplifier and bandpass filter are 48 µW and 660 µW, respectively, and the input-referred noise of the amplifier is 260 $\frac{\mathbf{V^2}}{\mathbf{Hz}}$.

One of the key challenges in the preamplifier design was achieving low-frequency response down to below 1 kHz, which was addressed using a pseudo-resistor. This pseudo-resistor provides a resistance of 7.95 GΩ, which, combined with a 0.1 µF capacitor, can establish a low-frequency cutoff of 150 Hz, which is crucial for capturing brain signals. Additionally, by considering appropriate bias current and values of gm, CL, and the midband gain, we have tuned the upper cutoff frequency of the preamplifier to 520 Hz, ensuring that the brain signals in the range of 80 µV to 2 mV are properly amplified. The preamplifier gain is designed to be around 40 dB, and the RFC amplifier stage provides an additional gain of 27.72 dB, ensuring adequate overall amplification. The designed system can be realized on a medical integrated circuit, and by incorporating a suitable ADC, it can provide a means to digitize the neural signals for further processing and analysis.

Declaration

We acknowledge that we used ChatGPT to enhance the academic writing of our manuscript while ensuring the originality and integrity of our work.

Transparency Statement

The data supporting this study are available upon reasonable request to the corresponding author, subject to ethical and confidentiality considerations.

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Declaration of Interest

The authors declare that they have no competing interests.

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